The Tractability Border of Reachability in Simple Vector Addition Systems with States

Henry Sinclair-Banks

Based on work with Dmitry Chistikov, Wojciech Czerwiński, Filip Mazowiecki, Łukasz Orlikowski, and Karol Węgrzycki to appear in FOCS'24.







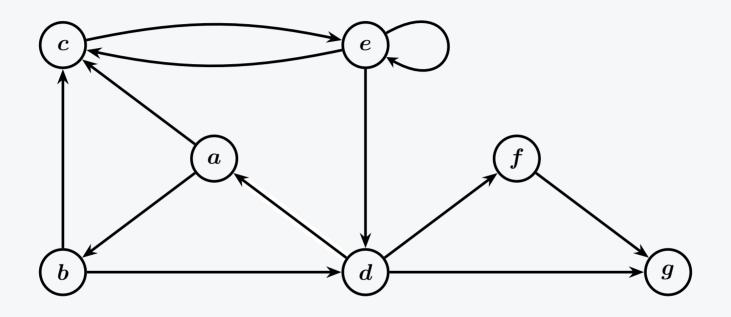




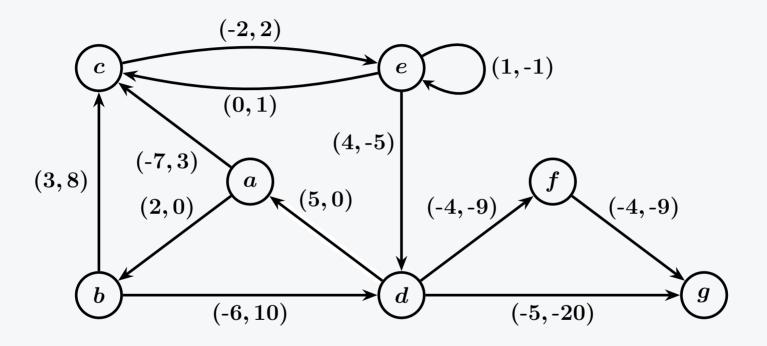


Algorithms & Complexity Seminar
27th August 2024
KIT, Karlsruhe, Germany

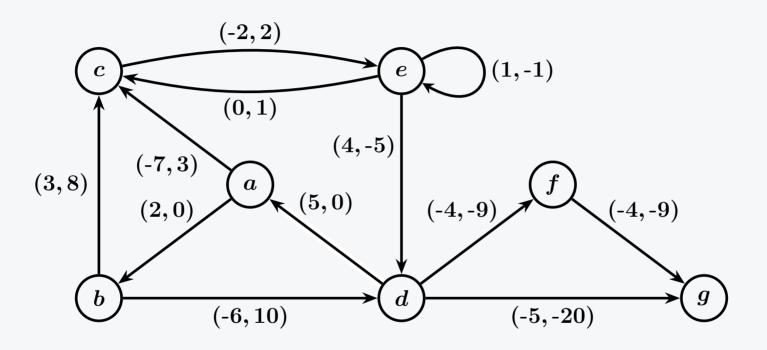
2-Dimensional Vector Addition System with States

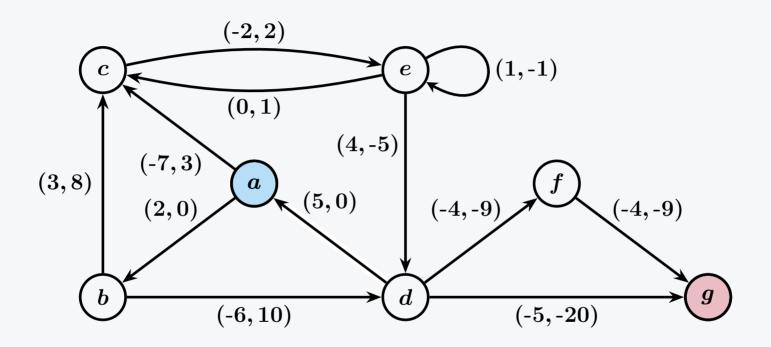


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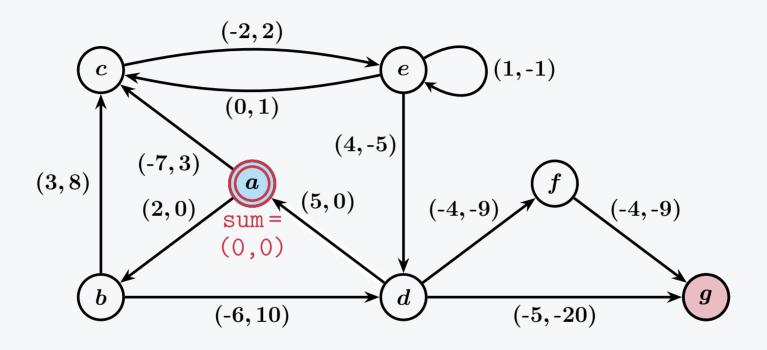


2-Dimensional VASS

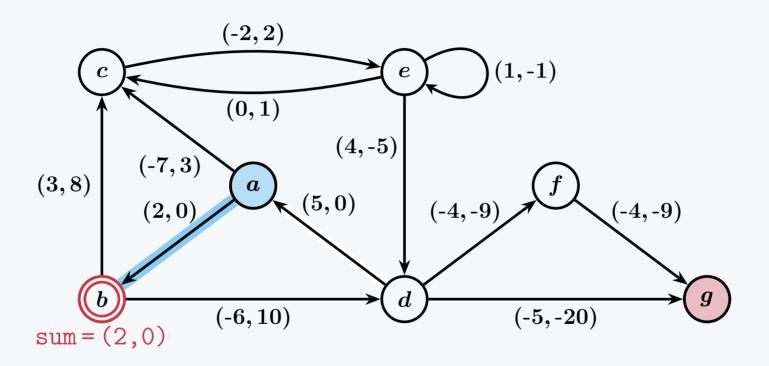




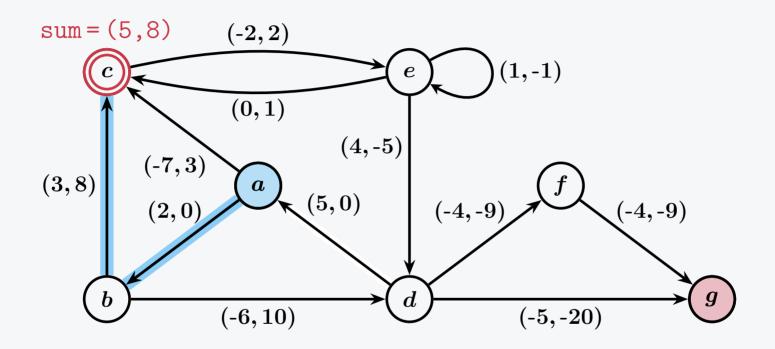
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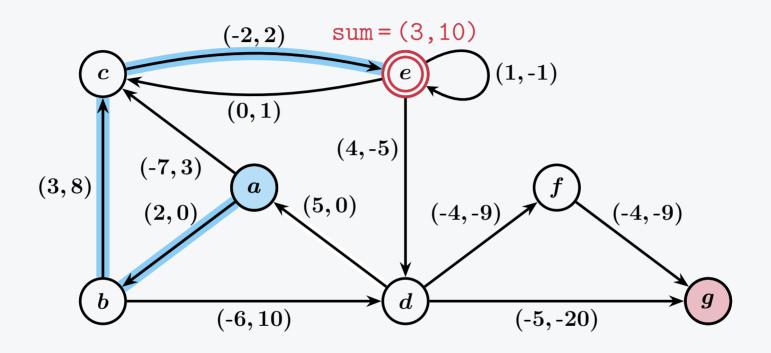
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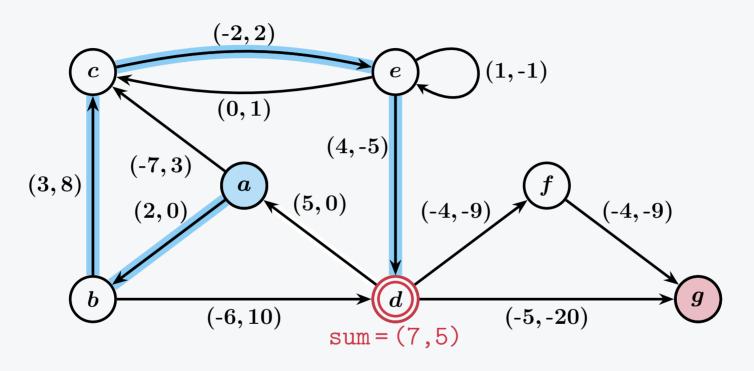
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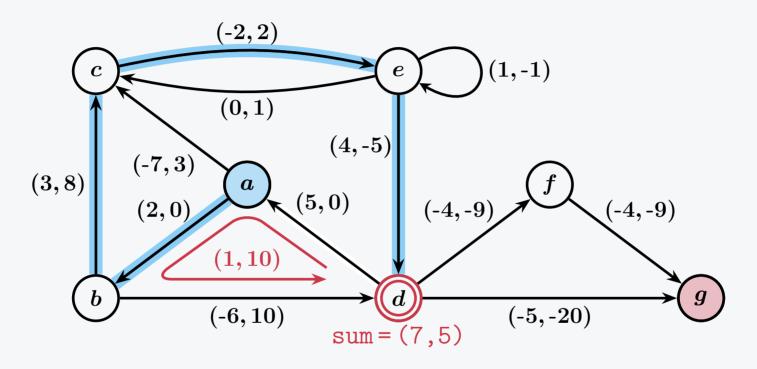
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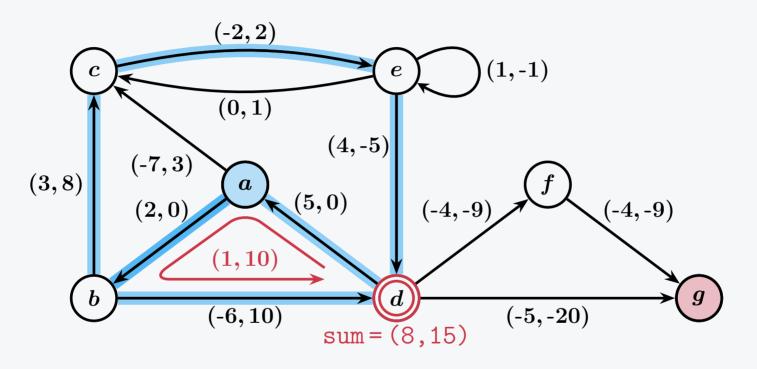
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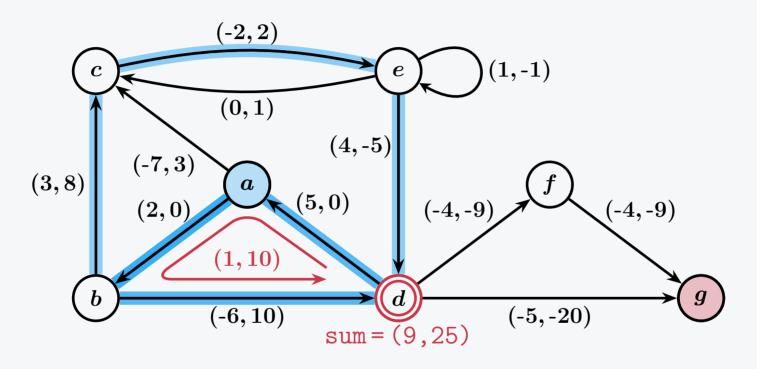
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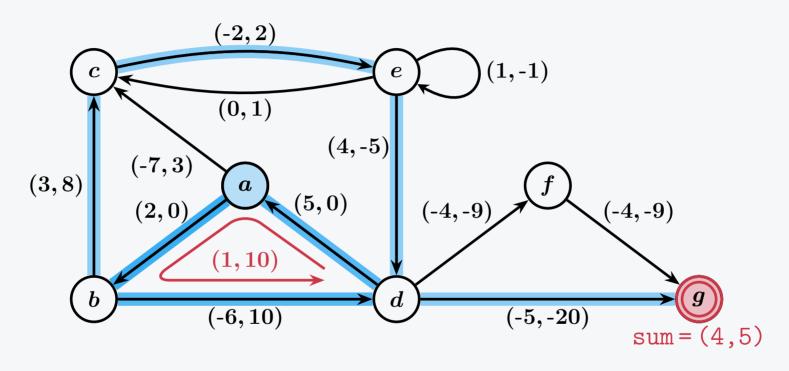
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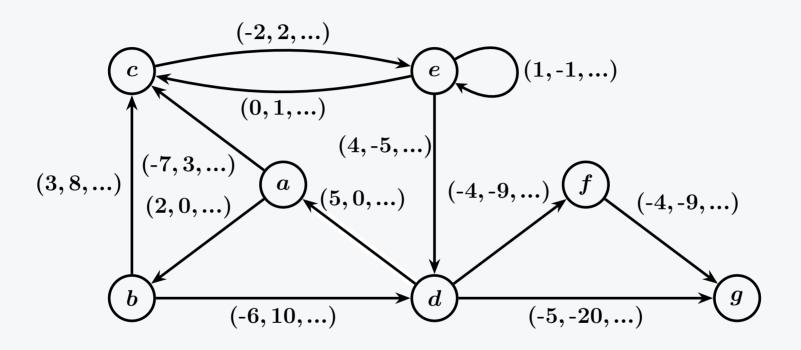


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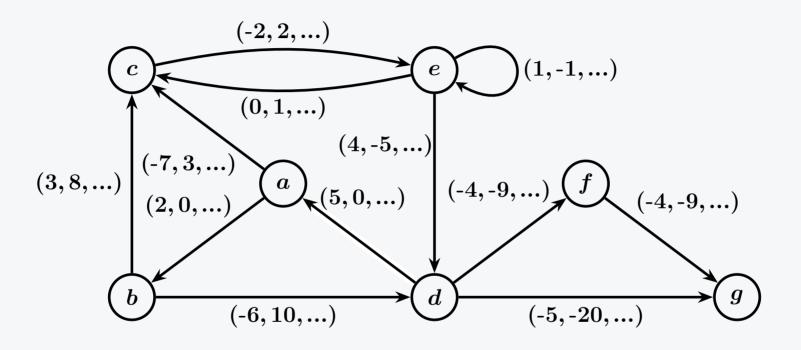


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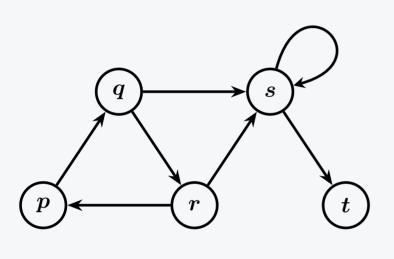
Reachability in VASS

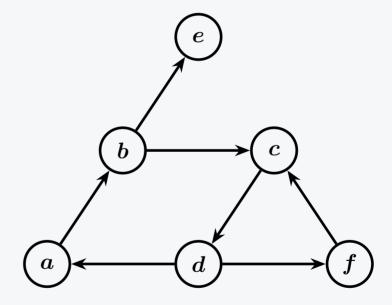


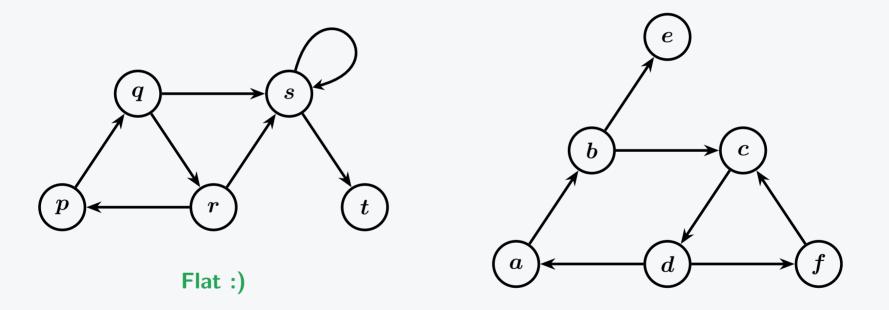
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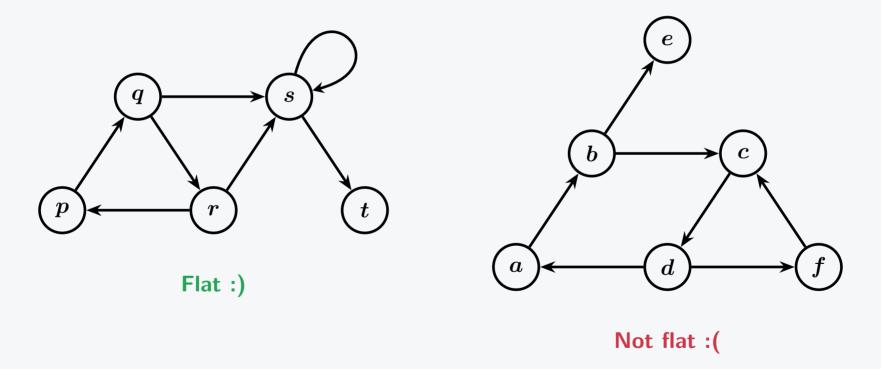


Reachability problem: does there exist a run from p(u) to q(v)?









Definition (Flat). For every state $q \in Q$, there is at most one simple cycle that contains q.

Theorem. Reachability in flat VASS is in NP (even with binary encoding). [Fribourg and Olsén '97]

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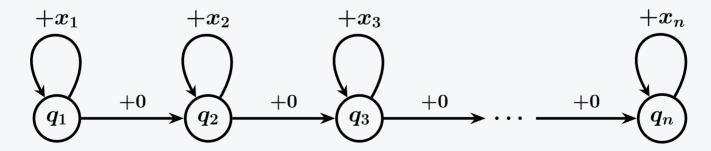
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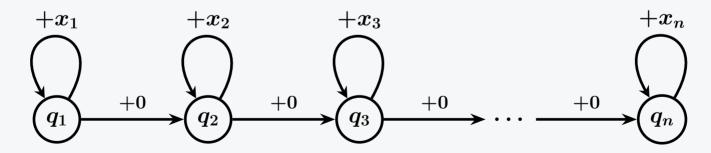
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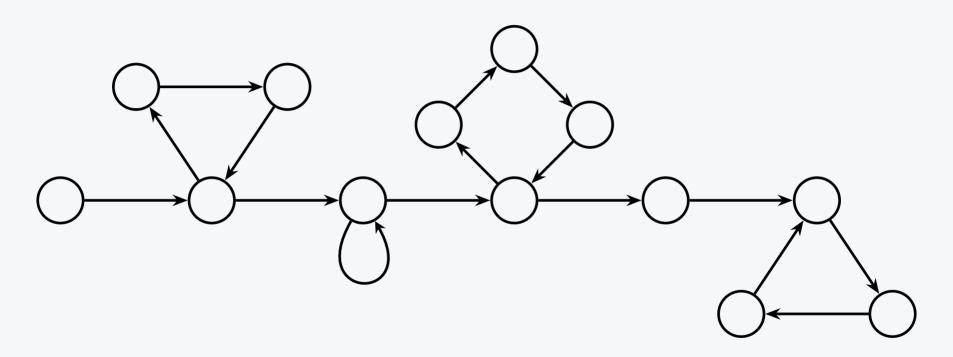
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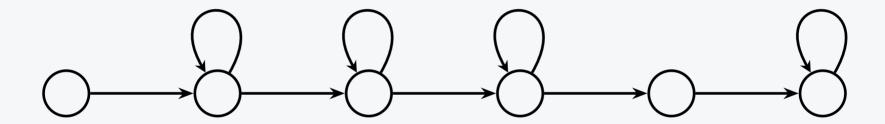
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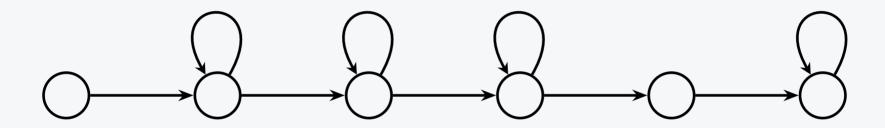
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For $d \geq 3$, is reachability in unary d-dimensional linear path schemes in P?

[Englert, Lazić, and Totzke '16]

[Leroux '21]

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Proof approach. Reduce from 3-SAT. Suppose φ has k variables (x_1,\ldots,x_k) and m clauses.

1) Use "Chinese remainder encoding" for SAT.

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 - Let p_1, \ldots, p_k be the first k primes.
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 - To verify that $n \equiv 0 mod p_i$ OR $n \equiv 1 mod p_i$, check $p_i \mid n$ OR $p_i \mid n-1$.
 - Instead, check $p_i \not\mid n-2$ AND $p_i \not\mid n-3$ AND \cdots AND $p_i \not\mid n-(p_i-1)$.

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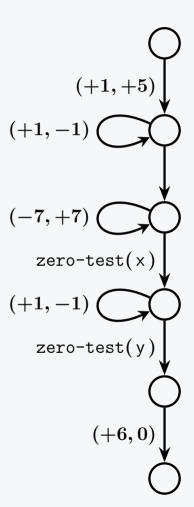
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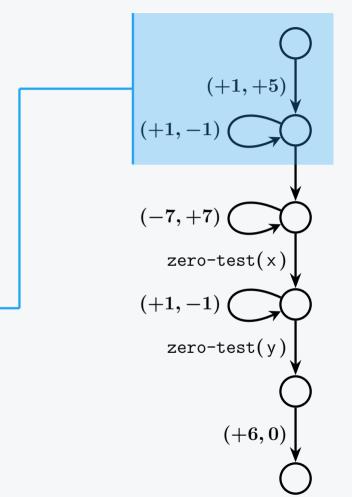
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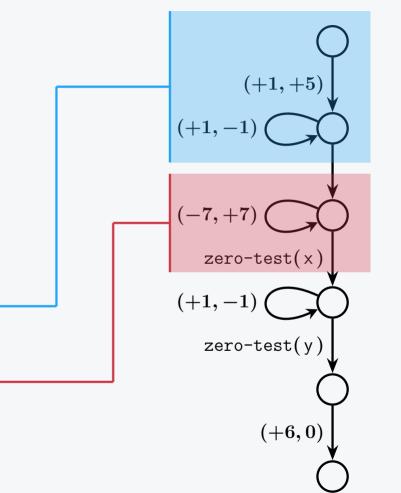
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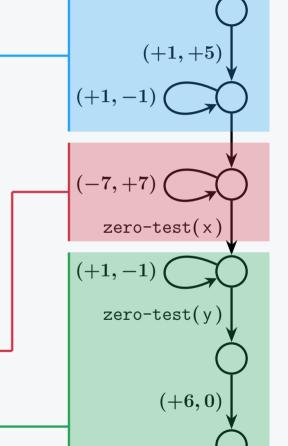
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- (iii) Restore x = v, y = 0.



Simulating Zero Tests

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Lemma 2.2 (Controlling Counter Technique). Let \mathcal{Z} be a d-VASS with zero tests and let $s(\mathbf{x}), t(\mathbf{y})$ be two configurations. Suppose \mathcal{Z} has the property that on any accepting run from $s(\mathbf{x})$ to $t(\mathbf{y})$, at most m zero tests are performed on each counter. Then there exists a (d+1)-VASS \mathcal{V} and two configurations $s'(\mathbf{0}), t'(\mathbf{y}')$ such that:

- (1) $s(\mathbf{x}) \stackrel{*}{\to}_{\mathcal{Z}} t(\mathbf{y})$ if and only if $s'(\mathbf{0}) \stackrel{*}{\to}_{\mathcal{V}} t'(\mathbf{y}')$,
- (2) V can be constructed in $\mathcal{O}((size(\mathcal{Z}) + ||x||) \cdot (m+1)^d)$ time, and
- $(3) \|\mathbf{y}'\| \leq \|\mathbf{y}\|.$

Moreover, if Z is a flat VASS or a (simple) linear path scheme in which no zero-testing transition lies on a cycle, then V can be assumed to be a flat VASS or a (simple) linear path scheme, respectively.

[Czerwiński and Orlikowski '21] [Chistikov, Czerwiński, Mazowiecki, Orlikowski, S., and Węgrzycki '24]

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Takeway message: A "small" number of zero tests can be simulated by an additional counter.

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- Obtain an equivalent conjunction of non-divisibility tests.

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- Use the controlling counter technique to obtain unary 3-SLPS for the SAT instance.

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Thank You!



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