3D Diamond Structures for Extreme Environment Logic

Whilst silicon based electronic systems have revolutionised the world around us, they are limited to operating in benign environments. There are a large number of high value applications, such as aerospace and nuclear, that require electronic systems that can operate in ambients that include temperatures beyond 300°C, the so called 'extreme environments'. Whilst the move to wide bandgap semiconductors is an enabling technology for the realisation of transistors for high temperature applications, significant challenges remain. High performance electronic circuits require transistors with short gate lengths and this results in a significant increase in the off state current, especially when the temperature is increased significantly above room temperature. This is often described as the lack of 'electrostatic integrity' for the transistor. The move to a 3D structure enhances the integrity of the device, resulting in an appreciable decrease in the off state current at high temperatures, as well as an increased current in the on state, and offers the possibility of a significant step change in capability for high temperature electronic devices.

Control of the surface of the diamond under the dielectric is a critical metric for the realisation of MOSFET structures and so the first mini-project will give the student experience in the characterisation of surfaces. During the main research activity, the use of surface engineering techniques, such as the use of atomically thin metal oxides at the interface between the diamond and the main dielectric will be investigated. Simulations performed at Newcastle have shown that it is possible to control the work function of the diamond surface and similar techniques in silicon carbide processing have shown that similar layers can be used to control the behaviour of the interface formed between the semiconductor and the gate dielectric.

The project will also investigate the quality of the diamond - dielectric interface using capacitance techiques. The difficulty in forming an inversion layer at the interface (a critical component in a MOSFET) has been described in terms of the density of interface traps (Dit). However, no measurements have been performed to extract Dit under inversion conditions, which are fundamental to gaining a full understanding of the MOSFET operation. Using a novel test structure that has been developed for silicon carbide technology, we will make the first measurements of Dit for diamond MOSFETs, investigating the influence of the different crystallographic planes that exist for a 3D structure and correlate this with the behaviour of the final MOSFET. The characterisation of diamond FETs will be supported by the second mini-project at Glasgow, working on the characterisation of high frequency diamond FETs.

The primary aim is to train the student in the development of diamond electronics and to generate knowledge in regard to the behaviour of the diamond - dielectric interface and routes to control of the key properties. In the longer term (beyond the end of the project) these outcomes will be exploited to develop logic circuits for extreme environments, where conventional silicon based technology cannot function.

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