UNIVERSITY OF WARWICK

Proposal Form for New or Revised Modules (MA1 - version 7 - April 2014)

Approval information	
Approval Type	☐ New module ☒ Revised module ☐ Discontinue module
Date of Introduction/Change	01/10/2016
If new, does this module replace another? If so, enter module code and title:	
If revised/discontinued, please outline the rationale for the changes:	To align documentation with module content that has been updated over the last decade.
Confirmation that affected departments have been consulted:	Computer Science Department informed.

Module Summary	
1. Module Code (if known)	ES3A3
2. Module Title	Analogue Systems Design
3a. Lead department:	Engineering
3b. Teaching Split (if known):	
4. Name of module leader	To be decided
5. Level	UG: ☐ Level 4 (Certificate) ☐ Level 5 (Intermediate) ☒ Level 6 (Honours) PG: ☐ Level 7 (Masters) ☐ Level 8 (Doctoral) See Guidance Notes for relationship to years of study
6. Credit value(s) (CATS)	15
7. Principal Module Aims	The module is designed to provide students with the ability to analyse and design analogue electronics.
8. Principal Learning Outcomes	At the end of the module the student should be able to 1. recognise and/or apply different circuit topologies to implement a variety of analogue functions 2. understand practical issues associated with the selection of

Module Summary	
	components 3. use models of components to analyse the nominal/or idealised behaviour of circuits 4. determine worse-case behaviour by use of software simulation tools and/or mathematical analysis 5. design analogue electronics 6. optimise circuit performance against a variety of criteria
9. Timetabled Teaching Activities (summary)	Lectures (20 x 1hr) spread evenly over one 10-week term Seminars (5 x 1hr) Laboratories (3 x 2hrs) Revision classes (2 x 1hr)
10. Departmental Web-link	http://www2.warwick.ac.uk/fac/sci/eng/eso/modules/year3/es3a3
11. Other essential notes	To enhance learning opportunities, guided pre-module preparation may be recommended to students who elect to take this module as part of a programme leading to a degree in General Engineering. Office hours are arranged for answering questions on the lecture material (theory and examples) and past examination questions.
12. Assessment methods (summary)	Assignment 20% Laboratory Report 10% 3 hours examination (70%)

For use by Strategic Planning and Analytics Office only - Do not fill in this section

Level	JACS3 Code	Teaching Split
		If not provided in 3b above

External Credit Level		Scheme	

Module Context

13. Please list all departments involved in the teaching of this module. If taught by more than one department, please indicate percentage split.

School of Engineering

14. Availability of module

Degree Code	Title	Study Year	C/OC/ A/B/C	Credits
H106	BEng Engineering	3	O	15
H107	MEng Engineering (and variants)	3	O	15
H109	MEng Engineering with intercalated year	3	O	15
H109	MEng Engineering with year in research	3	O	15
H634	BEng Electronic Engineering	3	C	15
H635	MEng Electronic Engineering (and variants)	3	C	15
H636	MEng Electronic Engineering with intercalated year	3	C	15
H637	MEng Engineering with year in research	3	C	15
G406	BEng Computer Systems Engineering	2	C	15
G408	MEng Computer Systems Engineering	2	C	15

15a. Minimum number of registered students required for module to run	1
15b. Maximum number permitted with suggested delivery and assessment strategies	90
16. Pre- and Post-Requisite Modules	None

Module Content and Teaching

17. Teaching and Learning Activities *(totals for module – please see guidance)*

Module duration (weeks)	10
Lectures	20 x 1 hour
Seminars	5 x 1 hour
Tutorials	
Project Supervision	
Demonstration	
Practical Class/Workshops	Laboratories (3x 2hrs).
Supervised time in studio/workshop	
Fieldwork	
External visits	
Work based learning	

Module Content and Teaching		
Placement		
Year abroad		
Other activity *(please describe): e.g. distance-learning, intensive weekend teaching etc.*	2 x 1-hour revision classes Self-study 117 hours.	
18. Assessment Method (Standard)		
Type of assessment	**Length**	**% weighting**
Written Examinations	Hours - 3	70%
Practical Examinations		
Assessed essays/coursework	Laboratory Report Assignment - Circuit design	10% 20%
18a. Final chronological assessment *(please see guidance*)	Examination	

19. Methods for providing feedback on assessment.

Individual feedback on assessed work.
Generic comments on submitted assessed work.
Model solutions to past examination papers are provided.

20. Outline Syllabus

Diodes, BJTs and FETs transistors
Analogue Circuit Modelling and Simulation
Behaviour of discrete capacitors
Voltage and current references
Digital to Analogue and Analogue to Digital Converters
Operational Amplifiers (including internal topology)
Filters
Signal Selection, processing and conversion (including multiplexing, ADC and DAC converters)
Comparators
Oscillators
Waveform Generators
Phase Locked Loops
Non-linear functions
Power management
Worst Case Design Analysis / Failure Modes and Effects Analysis

21. Illustrative Bibliography

1. "Microelectronic Circuits", Sedra and Smith, 2011, ISBN 9780199738519, TK 7835.S3
2. "Analysis and design of analog integrated circuits", Gray, H, 2009, ISBN 9780470398777, TK 7872.468.G7

22. Learning outcomes

Successful completion of the module leads to the learning outcomes. The learning outcomes identify the knowledge, skills and attributes developed by the module.

Learning Outcomes should be presented in the format "By the end of the module students should be able to..." using the table at the end of the module approval form:

Please see the table at the end of the module approval form.

Resources

23. List any additional requirements and indicate the outcome of any discussions about these.

Approval

24. Module leader's signature	Dr Christos Mias (as Discipline Degree Leader)
25. Date of approval	14 April 2016
26. Name of Approving Committee (include minute reference if applicable)	School of Engineering Teaching Policy Committee Meeting of 14 April 2016
27. Chair of Committee's signature	Dr David Dyer
28. Head of Department's signature	Professor Nigel Stocks

Examination Information		
A1. Name of examiner (if different from module leader)		
A2. Indicate all available methods of assessment in the table below		
% Examined	**% Assessed by other methods**	**Time of examination paper**
70	**30**	**3 hours**
A3. Will this module be examined together with any other module (sectioned paper)? If so, please give details below.		
A4. How many papers will the module be examined by?	☒ 1 paper	☐ 2 papers
A5. When would you wish the exam take place (e.g. Jan, April, Summer)?	**Summer**	
A6. Is reading time required?	☐ Yes	☒ No
A7. Please specify any special exam timetable arrangements.		
This will be a technical examination and it would be onerous to provide a separate paper for the second year students taking the paper if numbers dictated that this would be required.		
A8. Stationery requirements		
No. of Answer books?	**1**	
Graph paper?	**No**	
Calculator?	**Yes**	
Any other special stationery requirements (e.g. Data books, tables etc)?	**Engineering Data Book**	
A9. Type of examination paper		
Seen?	☐ Yes	☒ No
Open Book?	☐ Yes	☒ No
Restricted?	☐ Yes	☒ No
If restricted, please provide a list of permitted texts:		

LEARNING OUTCOMES		
(By the end of the module the student should be able to....)	**Which teaching and learning methods enable students to achieve this learning outcome? (reference activities in section 17)**	**Which summative assessment method(s) will measure the achievement of this learning outcome? (reference activities in section 18)**
1. Recognise and/or apply different circuit topologies to implement a variety of analogue functions	Lectures, guided personal study, formative exercises.	Written examination
2. Understand practical issues associated with the selection of components	Lectures, guided personal study, formative exercises.	Written examination
3. Use models of components to analyse the nominal/or idealised behaviour of circuits	Lectures, guided personal study, laboratory experiments, formative exercises.	Written examination
4. Determine worse-case behaviour by use of software simulation tools and/or mathematical analysis	Laboratory experiments, formative exercises.	Laboratory Report, Assignment and/or written examination
5. Design analogue electronics	Lectures, guided personal study, formative exercises.	Assignment Written examination
6. Optimise circuit performance against a variety of criteria	Lectures, guided personal study, formative exercises.	Assignment