UNIVERSITY OF WARWICK

Proposal Form for New or Revised Modules (MA1 - version 7 - April 2014)

Approval information	
Approval Type	☐ New module ☒ Revised module ☐ Discontinue module
Date of Introduction/Change	01/10/2018
If revised/discontinued, please outline the rationale for the changes:	Small changes to add new textbook and revise number of weeks.
Confirmation that affected departments have been consulted:	Changes were made in consultations between the School of Engineering and WMG.

Module Summary	
1. Module Code (if known)	ES2C4
2. Module Title	Computer Architecture and Systems
3a. Lead department:	School of Engineering
3b. Teaching Split (if known):	100% School of Engineering
4. Name of module leader	Suhaib A Fahmy
5. Level	UG: ☐ Level 4 (Certificate) ☒ Level 5 (Intermediate) ☐ Level 6 (Honours) PG: ☐ Level 7 (Masters) ☐ Level 8 (Doctoral) See Guidance Notes for relationship to years of study
6. Credit value(s) (CATS)	15
7. Principal Module Aims	To provide practical knowledge of how digital computing systems are designed, how they function, and how to program them.
8. Principal Learning Outcomes	By the end of the module the student should be able to: • Represent different types of data in binary and perform arithmetic operations on them. • Explain how low-level instructions correspond to the operation of a processor microarchitecture and how

Module Summary	
	complex programs can be decomposed into such instructions. • Explain the functionality of the basic components in a processor architecture. • Explain how external peripherals and memory are interfaced with a processor through a variety of interfaces. • Write microcontroller programs in C that go beyond a single iteration loop, taking advantage of interrupts and timers, and communicating with external peripherals.
9. Timetabled Teaching Activities (summary)	Lectures (20 x 1hr) Laboratories (6 x 2hrs) Revision Classes (2 x 1hr) **Total 34 hours**
10. Departmental Web-link	www2.warwick.ac.uk/fac/sci/eng/eso/modules/year2
11. Other essential notes	Advice and feedback hours for answering questions on the lecture material (theory and examples) and past examination questions. Guided reading and online tutorial material to be accessed in advance of module commencement. Laboratories support the design assignments.
12. Assessment methods (summary)	Two design assignments (20% each) with code and report submitted. 60% 2 hour examination Pass coursework overall at 30%.

For use by Strategic Planning and Analytics Office only - Do not fill in this section

Level	JACS3 Code	Teaching Split
		If not provided in 3b above

External Credit Level		Scheme	

Module Context

13. Please list all departments involved in the teaching of this module. If taught by more than one department, please indicate percentage split.

School of Engineering (100%)

14. Availability of module

Degree Code	Title	Study Year	C/OC/ A/B/C	Credits
H113	BEng Engineering	2	A/B	15
H114	MEng Engineering	2	A/B	15
H161	BEng Biomedical Systems Engineering	2	A	15
H163	MEng Biomedical Systems Engineering	2	A	15
H216	BEng Civil Engineering	2	A	15
H217	MEng Civil Engineering	2	A	15
H605	BEng Electrical and Electronic Engineering	2	C	15
H606	MEng Electrical and Electronic Engineering	2	C	15
H63W	BEng Electronic Engineering	2	C	15
H63X	MEng Electronic Engineering	2	C	15
HH35	BEng Systems Engineering	2	A	15
HH31	MEng Systems Engineering	2	A	15
HN11	BSc Engineering and Business Studies	2	A/B	15

15. Minimum number of registered students required for module to run

1 (core module).

16. Pre- and Post-Requisite Modules

Module Content and Teaching

17. Teaching and Learning Activities *(totals for module – please see guidance)*

Module duration (weeks)	10
Lectures	20×1hr = 20 hours
Seminars	
Tutorials	
Project Supervision	0
Demonstration	0
Practical Class/Workshops	6 × 2hr = 12 hours (supervised labs to support the design assignments)
Supervised time in studio/workshop	0
Fieldwork	0

Module Context		
External visits	0	
Work based learning	0	
Placement	0	
Year abroad	0	
Other activity *(please describe): e.g. distance-learning, intensive weekend teaching etc.*	2 x 1hr Revision Classes 116 hours of guided independent learning	
18. Assessment Method (Standard)		
Type of assessment	**Length**	**% weighting**
Written Examinations	2 hours	60
Practical Examinations		
Assessed essays/coursework	Two design assignments (8 page each)	40 (2 x 20%)
18a. Final chronological assessment *(please see guidance*)	Examination (60%)	
19. Methods for providing feedback on assessment.		

- Support through advice and feedback hours.
- Written feedback on marked programming assignments.
- Cohort-level feedback on final exam.

20. Outline Syllabus

Data Representation: Binary numbers, Boolean algebra, unsigned and signed integers, fixed and floating point, codes.
Logic and Digital Arithmetic: Basic function truth tables, multiplexers, encoders, decoders, half and full adders, multipliers, comparators and division.
Instruction Set Architecture: Assembly language, machine instructions including register, immediate, and jump, addressing modes, program flow.
Processor Microarchitecture: Memory, ALU, program counter, register file, control unit, single-cycle and pipelined processors.
Memory and I/O: Caches, virtual memory, GPIO, UART, RS232/485, SPI, I2C, high speed serial, timers, interrupts, PWM.
Microcontroller Programming: Basic C, loops, tasks, interrupts, accessing peripherals.

21. Illustrative Bibliography

- D. Harris and S. Harris. Digital Design and Computer Architecture. 2nd Edition. Publisher: Morgan Kaufmann, 2012, Paperback: 712 pages, ISBN-10: 0123944244, ISBN-13: 978-0123944245.

Module Context

- A. G. Dean, Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers, Arm Education Media UK, ISBN 978-1911531036.
- M. R. Mano, C. R. Kime, and T. Martin, Logic and Computer Design Fundamentals, 5th Ed, Pearson 2015. ISBN 978-1292096070

22. Learning outcomes

Successful completion of the module leads to the learning outcomes. The learning outcomes identify the knowledge, skills and attributes developed by the module.

Learning Outcomes should be presented in the format "By the end of the module students should be able to..." using the table at the end of the module approval form:

Please see the table at the end of the module approval form.

Resources

23. List any additional requirements and indicate the outcome of any discussions about these.

None

Approval	
24. Module leader's signature	Dr Suhaib Fahmy
25. Date of approval	20 March 2018
26. Name of Approving Committee (include minute reference if applicable)	School of Engineering and WMG Course and Module Approval Committee Minute 154-17/18
27. Chair of Committee's signature	Professor Gillian Cooke
28. Head of Department(s) signature	Professor David Towers

Examination Information		
A1. Name of examiner (if different from module leader)		
A2. Indicate all available methods of assessment in the table below		
% Examined	**% Assessed by other methods**	**Length of examination paper**
60	20% Design Assignment 1 20% Design Assignment 2	2 hours
A3. Will this module be examined together with any other module (sectioned paper)? If so, please give details below.		
No		
A4. How many papers will the module be examined by?	☒ 1 paper	☐ 2 papers
A5. When would you wish the exam take place (e.g. Jan, April, Summer)?	Summer	
A6. Is reading time required?	☐ Yes	☒ No
A7. Please specify any special exam timetable arrangements.		
A8. Stationery requirements		
No. of Answer books?	1	
Graph paper?	No	
Calculator?	Yes	
Any other special stationery requirements (e.g. Data books, tables etc)?	Engineering Data Book	
A9. Type of examination paper		
Seen?	☐ Yes	☒ No
Open Book?	☐ Yes	☒ No
Restricted?	☐ Yes	☒ No
If restricted, please provide a list of permitted texts:		

LEARNING OUTCOMES		
(By the end of the module the student should be able to....)	**Which teaching and learning methods enable students to achieve this learning outcome? (reference activities in section 15)**	**Which summative assessment method(s) will measure the achievement of this learning outcome? (reference activities in section 16)**
Represent different types of data in binary and perform arithmetic operations on them.	Lectures, laboratories.	Examination, design assignments.
Explain how low-level instructions correspond to the operation of a processor microarchitecture and how complex programs can be decomposed into such instructions.	Lectures.	Examination.
Explain the functionality of the basic components in a processor architecture.	Lectures, laboratories.	Examination, design assignments.
Explain how external peripherals and memory are interfaced with a processor through a variety of interfaces.	Lectures, laboratories.	Examination.
Write microcontroller programs in C that go beyond a single iteration loop, taking advantage of interrupts and timers, and communicating with external peripherals.	Lectures, laboratories.	Examination, design assignments.