UNIVERSITY OF WARWICK

Proposal Form for New or Revised Modules (MA1 - version 7 - April 2014)

Approval information	
Approval Type	☐ New module ☒ Revised module ☐ Discontinue module
Date of Introduction/Change	October 2018
If new, does this module replace another? If so, enter module code and title:	
If revised/discontinued, please outline the rationale for the changes:	Revised to increase design assignment weighting, shorten exam.
Confirmation that affected departments have been consulted:	

Module Summary	
1. Module Code (if known)	ES3B2
2. Module Title	Digital Systems Design
3a. Lead department:	Engineering
3b. Teaching Split (if known):	100% Engineering
4. Name of module leader	Suhaib A Fahmy
5. Level	UG: ☐ Level 4 (Certificate) ☐ Level 5 (Intermediate) ☒ Level 6 (Honours) PG: ☐ Level 7 (Masters) ☐ Level 8 (Doctoral) See Guidance Notes for relationship to years of study
6. Credit value(s) (CATS)	15
7. Principal Module Aims	To introduce students to the principles and practice of designing digital electronic circuits, with a focus on field programmable gate array implementation, including the tool flow, architecture, testing, and design for performance.

Module Summary	
8. Principal Learning Outcomes	By the end of the module students will be able to: • Through the practical use of the Verilog hardware description language (HDL), consolidate understanding of the theory of combinational and sequential circuits and how these combine in the design of digital computing circuits. • Evaluate the digital design flow as currently practised professionally in industry, with reference to field programmable gate arrays, and at a more general level, to custom application specific integrated circuits. • Analyse how mathematics is performed in custom circuits, and how simple units can be combined to implement complex compute datapaths. • Devise a testing strategy and design a testbench to evaluate the functional correctness of a circuit using the testing features of the Verilog HDL and a professional standard simulator. • Reason about the performance of synchronous digital circuits, based on the timing of basic components, and how pipelining affects performance, and how this differs from measuring the performance of software running on processors.
9. Timetabled Teaching Activities (summary)	20 hrs lectures 7 x 2hr laboratories (un-assessed, support design assignment) 2 x 1 hr revision classes **Total 36 hours**
10. Departmental Web-link	http://www2.warwick.ac.uk/fac/sci/eng/eso/modules/year3/es3b2
11. Other essential notes	Advice and feedback hours for answering questions on the lecture material (theory and examples) and past examination questions.
12. Assessment methods (summary)	40% Assessed Design Assignment (10 pages report) 60% Examination (2 hour) Student must pass the examination and the coursework.

For use by Strategic Planning and Analytics Office only - Do not fill in this section

Level	JACS3 Code	Teaching Split
		If not provided in 3b above

External Credit Level		Scheme	

Module Context

13. Please list all departments involved in the teaching of this module. If taught by more than one department, please indicate percentage split.

Engineering

14. Availability of module

Degree Code	Title	Study Year	C/OC/ A/B/C	Credits
H634	BEng Electronic Engineering	3	C	15
H635	MEng Electronic Engineering and variants	3	C	
H636	MEng Electronic Engineering with Intercalated Year	3	C	
H637	MEng Electronic Engineering with Year in Research	3	C	
H106	BEng Engineering	3	O	
H107	MEng Engineering and variants	3	O	
H109	MEng Engineering with Intercalated Year	3	O	
H110	MEng Engineering with Year in Research	3	O	

15. Minimum number of registered students required for module to run

1 (core)

16. Pre- and Post-Requisite Modules

ES2C4 Computer Architecture and Systems

Module Content and Teaching

17. Teaching and Learning Activities *(totals for module – please see guidance)*

Module duration (weeks)	10
Lectures	20 × 1hr = 20 hrs
Seminars	0

Module Content and Teaching	
Tutorials	
Project Supervision	0
Demonstration	0
Practical Class/Workshops	7 × 2hr = 14 hrs (supervised labs)
Supervised time in studio/workshop	0
Fieldwork	0
External visits	0
Work based learning	0
Placement	0
Year abroad	0
Other activity *(please describe): e.g. distance-learning, intensive weekend teaching etc.*	Revision classes: 2 × 1 hr Guided independent learning: 114 hrs

18. Assessment Method (Standard)		
Type of assessment	**Length**	**% weighting**
Written Examinations	2 Hours	60
Practical Examinations	N/A	
Assessed essays/coursework	Assessed Design Assignment to design and implement a digital circuit of moderate complexity using the skills learnt in the course (10 pages report).	40
18a. Final chronological assessment *(please see guidance*)	Unseen examination	

19. Methods for providing feedback on assessment.

Detailed marking on assessed design exercise.
Model solutions are published for past examination papers
Cohort level feedback on examinations

20. Outline Syllabus

Recap of combinational and sequential circuits: gates, multiplexers, encoders, decoders, latches, D flip-flop, registers, shift registers.
Design with hardware description languages: (Verilog) module definitions, gate-level circuits, assign statements, behavioural combinational descriptions, behavioural synchronous descriptions.
Design flow and FPGA architecture: basic circuit synthesis, FPGA logic blocks, hard blocks, I/O, mapping to FPGA blocks, placement and routing, configuring FPGAs.
Testing digital circuits: basic Verilog testbenches, self-checking testbenches, file I/O for input/output vectors, testing strategies.

Module Content and Teaching

Arithmetic circuits: limits of ripple adders, carry-lookahead adders, multipliers, fixed-point data representation and resulting errors, floating point circuit complexity.
Timing and pipelining: basic combinational timing characteristics, timing of synchronous components, computing circuit timing performance, pipelining for improved performance, hazards, race conditions, and metastability.
Processors and I/O: basic structure of a processor and how this relates to performance, integrating peripherals over UART, SPI, I2C, and faster serial standards, computing data rates for these standards.

21. Illustrative Bibliography

- D. M. Harris and S. L. Harris, Digital Design and Computer Architecture, 2nd ed., Morgan Kaufmann, 2013. ISBN 978-0123944245
- S. Brown and Z. Vranseic, Fundamentals of Digital Logic with Verilog Design, 3rd ed., McGraw Hill, 2014. ISBN 978-0073380544

22. Learning outcomes

Successful completion of the module leads to the learning outcomes. The learning outcomes identify the knowledge, skills and attributes developed by the module.

Learning Outcomes should be presented in the format "By the end of the module students should be able to..." using the table at the end of the module approval form:

Please see the table at the end of the module approval form.

Resources

23. List any additional requirements and indicate the outcome of any discussions about these.

Approval	
24. Module leader's signature	Dr Suhaib A Fahmy
25. Date of approval	13/09/2018
26. Name of Approving Committee (include minute reference if applicable)	School of Engineering Course and Module Approval Committee
27. Chair of Committee's signature	Gill Cooke
28. Head of Department(s) signature	David Towers

Examination Information		
A1. Name of examiner (if different from module leader)		
A2. Indicate all available methods of assessment in the table below		
% Examined	**% Assessed by other methods**	**Length of examination paper**
60	40 Design Assignment	2 hours
A3. Will this module be examined together with any other module (sectioned paper)? If so, please give details below.		
No		
A4. How many papers will the module be examined by?	☒ 1 paper	☐ 2 papers
A5. When would you wish the exam take place (e.g. Jan, April, Summer)?	Summer	
A6. Is reading time required?	☐ Yes	☒ No
A7. Please specify any special exam timetable arrangements.		
Must be timetabled at the same time and in the same location as ES2E3 which is taken by the CSE students.		
A8. Stationery requirements		
No. of Answer books?	1	
Graph paper?	No	
Calculator?	Yes	
Any other special stationery requirements (e.g. Data books, tables etc)?	**Engineering Data Book**	
A9. Type of examination paper		
Seen?	☐ Yes	☒ No
Open Book?	☐ Yes	☒ No
Restricted?	☐ Yes	☒ No
If restricted, please provide a list of permitted texts:		

LEARNING OUTCOMES		
(By the end of the module the student should be able to....)	**Which teaching and learning methods enable students to achieve this learning outcome? (reference activities in section 15)**	**Which summative assessment method(s) will measure the achievement of this learning outcome? (reference activities in section 16)**
Through the practical use of the Verilog hardware description language (HDL), consolidate understanding of the theory of combinational and sequential circuits and how these combine in the design of digital computing circuits.	Lectures, problem sheets, laboratories, background reading.	Examination, assessed design exercise.
Evaluate the digital design flow as currently practised professionally in industry, with reference to field programmable gate arrays, and at a more general level, to custom application specific integrated circuits.	Lectures, problem sheets, laboratories, background reading.	Examination.
Analyse how mathematics is performed in custom circuits, and how arithmetic units can be combined to implement complex compute datapaths.	Lectures, problem sheets, laboratories, background reading.	Examination, assessed design exercise.
Devise a testing strategy and design a testbench to evaluate the functional correctness of a circuit using the testing features of the Verilog HDL and a professional standard simulator.	Lectures, problem sheets, laboratories, background reading.	Examination, assessed design exercise.
Reason about the performance of synchronous digital circuits, based on the timing of basic components, and how pipelining affects performance, and how this differs from measuring the performance of software running on processors.	Lectures, problem sheets, laboratories, background reading.	Examination, assessed design exercise.