UNIVERSITY OF WARWICK

Proposal Form for New or Revised Modules (MA1 - version 7 - April 2014)

Approval information	
Approval Type	☐ New module ☒ Revised module ☐ Discontinue module
Date of Introduction/Change	October 2018
If new, does this module replace another? If so, enter module code and title:	
If revised/discontinued, please outline the rationale for the changes:	Revised to increase the lecture hours from 15 to 20, to change the length of the design report, to make minor modifications to syllabus and learning outcomes without affecting the ticked IET learning outcomes.
Confirmation that affected departments have been consulted:	Changes have been made in consultation between the School of Engineering and WMG.

Module Summary	
1. Module Code (if known)	ES3D8
2. Module Title	Fundamentals of Modern VLSI Design
3a. Lead department:	Engineering
3b. Teaching Split (if known):	100% Engineering
4. Name of module leader	Dr Marina Cole
5. Level	UG: ☐ Level 4 (Certificate) ☐ Level 5 (Intermediate) ☒ Level 6 (Honours) PG: ☐ Level 7 (Masters) ☐ Level 8 (Doctoral) See Guidance Notes for relationship to years of study
6. Credit value(s) (CATS)	15
7. Principal Module Aims	The course aims to present the principles and techniques of digital VLSI design, connecting digital system and logic design with the fundamental device physics, processing techniques and transistor level characteristics of Silicon integrated circuits, both in theortical and practical aspects.

Module Summary	
8. Principal Learning Outcomes	By the end of the module students should be able to: • Examine how digital VLSI technology affects logic implementation and optimisation of simple CMOS integrated circuits. • Apply simplified models to estimate the delay and power consumption of digital integrated circuits. • Design digital logic circuits based on different circuit families with different trade-offs in speed, power, complexity and robustness. • Acquire skills in the use of Computer Aided Design Software for VLSI such as Tanner Tools or Cadence. • Use a variety of technologies, design and analysis techniques for implementation of digital VLSI systems. • Manage complex designs including partitioning into CMOS subsystems such as datapaths and memory arrays.
9. Timetabled Teaching Activities (summary)	20x1h lectures, 18 h (9x2h) labs, 1 h examples class **Total: 39 hours**
10. Departmental Web-link	http://www2.warwick.ac.uk/fac/sci/eng/eso/modules/year3/
11. Other essential notes	Advice and feedback hours are arranged for answering questions on the lecture material (theory and examples) and past examination questions.
12. Assessment methods (summary)	50% coursework (25% Design Report 1500 words plus 25% Electronic Submission of Designs) 50% 2 hour examination

For use by Strategic Planning and Analytics Office only - Do not fill in this section

Level	JACS3 Code	Teaching Split
		If not provided in 3b above

External Credit Level		Scheme	

Module Context

13. Please list all departments involved in the teaching of this module. If taught by more than one department, please indicate percentage split.

School of Engineering

14. Availability of module

Degree Code Up to 16-17 entry	**Title**	**Study Year**	**C/OC/ A/B/C**	**Credits**
H634	BEng Electronic Engineering	3	C	15
H63U	BEng Electronic Engineering with Intercalated Year	4	C	15
H635	MEng Electronic Engineering	3	C	15
H636	MEng Electronic Engineering with an Intercalated Year	3 or 4	C	15
H637	MEng Electronic Engineering with a Year in Research	3 or 4	C	15
H106	BEng Engineering	3	A	15
New	BEng Engineering with Intercalated Year	4	A	15
H107	MEng Engineering	3	A	15
H109	MEng Engineering with Intercalated Year	3 or 4	A	15
H110	MEng Engineering with a Year in Research	3 or 4	A	15
G406	BSc/BEng Computer Systems Engineering	3	A	15
G408	MEng Computer Systems Engineering	3	A	15
Degree Code From 17-18 entry	**Title**	**Study Year**	**C/OC/ A/B/C**	**Credits**
H63W	BEng Electronic Engineering	3	C	15
H63V	BEng Electronic Engineering with Intercalated Year	4	C	15
H63X	MEng Electronic Engineering	3	C	15
H63Y	MEng Electronic Engineering with an Intercalated Year	3 or 4	C	15
H113	BEng Engineering	3	A	15
H111	BEng Engineering with Intercalated Year	4	A	15
H114	MEng Engineering	3	A	15
H115	MEng Engineering with Intercalated Year	3 or 4	A	15

15. Minimum number of registered students required for module to run

1 (core module)

Module Context

16. Pre- and Post-Requisite Modules

ES434 ASICs, MEMs and Smart Devices

Module Content and Teaching

17. Teaching and Learning Activities *(totals for module – please see guidance)*

Module duration (weeks)	10
Lectures	20 x 1 hours
Seminars	0
Tutorials	1 x 1 hour examples class
Project Supervision	0
Demonstration	0
Practical Class/Workshops	9 x 2 hours
Supervised time in studio/workshop	0
Fieldwork	0
External visits	0
Work based learning	0
Placement	0
Year abroad	0
Other activity *(please describe): e.g. distance-learning, intensive weekend teaching etc.*	111 hours Guided Independent Learning

18. Assessment Method (Standard)

Type of assessment	**Length**	**% weighting**
Written Examinations	2 Hours	**50**
Practical Examinations		
Assessed essays/coursework	• Electronic Design • Written report related to Electronic design 1500 Words	**25** **25**
18a. Final chronological assessment *(please see guidance*)	**Exam**	

19. Methods for providing feedback on assessment.

Feedback on assessment is by individual feedback mark sheet and overview. Feedback will be provided during the last 4 laboratory sessions and for the written report.
Cohort level feedback on examinations

20. Outline Syllabus

Silicon Processing. CMOS circuits for logic gates. Cell layout styles. Cell composition and structured layout techniques. Transmission gate logic and dynamic memory. Latches. Complex CMOS gates. Dynamic logic. Timing analysis and optimisation. Logical Effort and Delay Estimation. Power dissipation. Sequential Logic Design. Subsystem design: adders, , RAM, datapath and PLA/ROM. Managing Complex Designs, Clocks, I/O, Packaging. Design Exercises to cover cell layout and composition, switch level simulation and timing analysis, critical path finding and circuit level simulation for timing and power.

21. Illustrative Bibliography

"Fundamentals of Modern VLSI Devices, Taur, Y, 2013, 978-1107635715
"Integrated Circuit Design", Weste, N.H.E, 2011, 978-0321696946
"CMOS VLSI design", Weste, N.H.E, 2011, 9780321547743, TK 7872.468.W3
"CMOS: Circuit Design, Layout, and Simulation", Baker, R.J, 2011, 9781118038239
"Modern VLSI Design", Wolf,W, 2009, 978-0137145003,

22. Learning outcomes

Successful completion of the module leads to the learning outcomes. The learning outcomes identify the knowledge, skills and attributes developed by the module.

Please, see the table at the end of the module approval form.

Resources

23. List any additional requirements and indicate the outcome of any discussions about these.

Site license for Tanner Tools or Cadence design software running on PCs to be provided as on the existing module.

Approval

24. Module leader's signature	Dr Marina Cole
25. Date of approval	25 April 2018
26. Name of Approving Committee (include minute reference if applicable)	School of Engineering and WMG Course and Module Approval Committee (CMAC), Minute 255-17/18.
27. Chair of Committee's signature	Professor Gillian Cooke
28. Head of Department(s) signature	Professor David Towers

Examination Information		
A1. Name of examiner (if different from module leader)		
A2. Indicate all available methods of assessment in the table below		
% Examined	**% Assessed by other methods**	**Length of examination paper**
50	25 Electronic Design 25 Written report related to Electronic design 1500 Words	**2**
A3. Will this module be examined together with any other module (sectioned paper)? If so, please give details below.		
No		
A4. How many papers will the module be examined by?	☒ 1 paper	☐ 2 papers
A5. When would you wish the exam take place (e.g. Jan, April, Summer)?	**Summer**	
A6. Is reading time required?	☐ Yes	☒ No
A7. Please specify any special exam timetable arrangements.		
N/A		
A8. Stationery requirements		
No. of Answer books?	**1**	
Graph paper?	**No**	
Calculator?	**Yes**	
Any other special stationery requirements (e.g. Data books, tables etc)?	**Engineering Data Book**	
A9. Type of examination paper		
Seen?	☐ Yes	☒ No
Open Book?	☐ Yes	☒ No
Restricted?	☐ Yes	☒ No
If restricted, please provide		

Approval	
a list of permitted texts:	

LEARNING OUTCOMES		
(By the end of the module the student should be able to....)	**Which teaching and learning methods enable students to achieve this learning outcome? (reference activities in section 15)**	**Which summative assessment method(s) will measure the achievement of this learning outcome? (reference activities in section 16)**
Examine how digital VLSI technology affects logic implementation and optimisation of simple CMOS integrated circuits.	Lecturing material, handouts and course textbook	Examination
Apply simplified models to estimate the delay and power consumption of digital integrated circuits.	Lecturing material, handouts and course textbook	Examination
Design digital logic circuits based on different circuit families with different trade-offs in speed, power, complexity and robustness.	Lecturing material and laboratories	Electronic designs and examination
Acquire skills in the use of Computer Aided Design Software for VLSI such as Tanner Tools or Cadence.	Laboratories	Electronic designs and reports
Use a variety of technologies, design and analysis techniques for implementation of digital VLSI systems.	Course material, course textbook, and lab sessions.	Electronic designs and reports
Manage complex designs including partitioning into CMOS subsystems such as datapaths and memory arrays.	Lecturing material, handouts, course textbook and lab sessions	Electronic designs