UNIVERSITY OF WARWICK

Proposal Form for New or Revised Modules (MA1 - version 7 - April 2014)

Approval information	
Approval Type	☒ New module ☐ Revised module ☐ Discontinue module
Date of Introduction/Change	October 2018
If new, does this module replace another? If so, enter module code and title:	Alternative code for ES4F3 (engineering students) Computer Systems Engineering where the module is taken in the 3rd year.
If revised/discontinued, please outline the rationale for the changes:	
Confirmation that affected departments have been consulted:	

Module Summary	
1. Module Code (if known)	ES3F1
2. Module Title	High Performance Embedded Systems Design
3a. Lead department:	School of Engineering
3b. Teaching Split (if known):	100% School of Engineering
4. Name of module leader	Dr Suhaib A Fahmy
5. Level	UG: ☐ Level 4 (Certificate) ☐ Level 5 (Intermediate) ☒ Level 6 (Honours) PG: ☐ Level 7 (Masters) ☐ Level 8 (Doctoral) See Guidance Notes for relationship to years of study
6. Credit value(s) (CATS)	15
7. Principal Module Aims	To develop a student's ability in digital design to the level of designing high performance software/hardware embedded systems using hybrid FPGA reconfigurable devices combining processors and reconfigurable hardware fabric.

Module Summary	
8. Principal Learning Outcomes	By the end of the module the student should be able to: • Apply the more advanced features of FPGA architectures in high performance embedded systems design. • Design a hardware accelerator for a complex algorithm by evaluating its parallelism and arithmetic requirements. • Integrate a hardware accelerator with a processor and design the necessary software and hardware communication infrastructure. • Apply practical knowledge of hardware design at the register transfer level and use high level synthesis.
9. Timetabled Teaching Activities (summary)	20 x 1 hour Lectures 7 x 2 hours Laboratories (un-assessed, support design assignment) 2 x 1 hour Revision Classes **Total 36 hours**
10. Departmental Web-link	www2.warwick.ac.uk/fac/sci/eng/eso/modules/year4
11. Other essential notes	Advice and feedback hours for answering questions on the lecture material (theory and examples) and past examination questions.
12. Assessment methods (summary)	40% Assessed Design Assignment (10 pages report) 60% Examination (2 hour) Student must pass the examination and the coursework.

For use by Strategic Planning and Analytics Office only - Do not fill in this section

Level	JACS3 Code	Teaching Split
		If not provided in 3b above

External Credit Level		Scheme	

Module Context

13. Please list all departments involved in the teaching of this module. If taught by more than one department, please indicate percentage split.

School of Engineering

14. Availability of module

Degree Code	Title	Study Year	C/OC/ A/B/C	Credits
G406	BEng Computer Systems Engineering	3	C	15
G408	MEng Computer Systems Engineering	3	C	15

15. Minimum number of registered students required for module to run

1 (Core)

16. Pre- and Post-Requisite Modules

ES2E3 Digital Systems Design

Module Content and Teaching

17. Teaching and Learning Activities *(totals for module – please see guidance)*

Module duration (weeks)	10
Lectures	20 × 1 hour
Seminars	
Tutorials	
Project Supervision	
Demonstration	
Practical Class/Workshops	7 × 2 hours (supervised labs)
Supervised time in studio/workshop	
Fieldwork	
External visits	
Work based learning	
Placement	
Year abroad	
Other activity *(please describe): e.g. distance-learning, intensive weekend teaching etc.*	2 x 1 hour Revision classes 114 hours Guided Independent Learning

Module Content and Teaching

18. Assessment Method (Standard)

Type of assessment	Length	% weighting
Written Examinations	2 Hours	60
Practical Examinations	N/A	
Assessed essays/coursework	Assessed design assignment to design and implement a digital circuit of advanced complexity using the skills learnt in the module (10 pages design report)	40
18a. Final chronological assessment *(please see guidance*)	Examination	

19. Methods for providing feedback on assessment.

- Support through office hours.
- Detailed marking on assessed design assignment.
- Cohort-level feedback on final exam.

20. Outline Syllabus

Verilog Recap. Datapath design, modelling computational units, verification with specialist software.
Modern Hybrid FPGA Architecture. Advanced DSP block architecture, advanced I/O, partial reconfiguration, hybrid FPGA architecture, PCIe-connected FPGAs.
Accelerating Algorithms. Finding performance bottlenecks, parallelising algorithms, pipelining, adding flexibility, number representations for arithmetic.
Design Space Exploration. Area-performance-power trade-offs.
High Level Synthesis. C-to-gates and other languages, compiler outline, supported language features, using compiler directives.
Integrating Software and Hardware. Processor to logic interfacing, streaming and programme I/O, blocking and non-blocking communication, managing reconfiguration.

21. Illustrative Bibliography

Embedded Systems Design with FPGAs, P Athanas, D. Pnevmatikatos, N. Sklavos (Editors), Springer, 2013.

Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers, A. G. Dean, Arm Education Media UK, 2017.
The Zynq Book: Embedded Processing with the ARM® Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, Strathclyde Academic Media, 2014

22. Learning outcomes
Please see the table at the end of the module approval form.

Resources

Module Content and Teaching
23. List any additional requirements and indicate the outcome of any discussions about these.
Expect a half matched donation of boards as for previous courses.

Approval	
24. Module leader's signature	Dr Suhaib A Fahmy
25. Date of approval	13/09/18
26. Name of Approving Committee (include minute reference if applicable)	CMAC Committee
27. Chair of Committee's signature	Gill Cooke
28. Head of Department(s) signature	David Towers

Examination Information		
A1. Name of examiner (if different from module leader)		
A2. Indicate all available methods of assessment in the table below		
% Examined	**% Assessed by other methods**	**Length of examination paper**
60%	40% Assessed Design Assignment (2000 words – excluding figures)	2 hours
A3. Will this module be examined together with any other module (sectioned paper)? If so, please give details below.		
No		
A4. How many papers will the module be examined by?	☒ 1 paper	☐ 2 papers
A5. When would you wish the exam take place (e.g. Jan, April, Summer)?	Summer	
A6. Is reading time required?	☐ Yes	☒ No
A7. Please specify any special exam timetable arrangements.		
A8. Stationery requirements		
No. of Answer books?	1	
Graph paper?	No	
Calculator?	Yes	
Any other special stationery requirements (e.g. Data books, tables etc)?	**Engineering Data Book**	
A9. Type of examination paper		
Seen?	☐ Yes	☒ No
Open Book?	☐ Yes	☒ No
Restricted?	☐ Yes	☒ No
If restricted, please provide a list of permitted texts:		

LEARNING OUTCOMES		
(By the end of the module the student should be able to....)	**Which teaching and learning methods enable students to achieve this learning outcome? (reference activities in section 15)**	**Which summative assessment method(s) will measure the achievement of this learning outcome? (reference activities in section 16)**
Apply advanced features of FPGA architectures in high performance embedded systems design.	Lectures, problem sheets, laboratories.	Examination, assessed design assignment.
Design a hardware accelerator for a complex algorithm by evaluating its parallelism and arithmetic requirements.	Lectures, problem sheets, laboratories.	Examination, assessed design assignment.
Integrate a hardware accelerator with a processor and design the necessary software and hardware communication infrastructure.	Lectures, problem sheets, laboratories.	Examination, assessed design assignment.
Apply practical knowledge of hardware design at the register transfer level and understand the principles of high level synthesis.	Lectures, problem sheets, laboratories.	Examination, assessed design assignment.
Understand the trade-offs between performance, area, and power in the design of accelerators.	Lectures, problem sheets, laboratories.	Examination.