Hafnium oxide: A thin film dielectric with controllable etch resistance for semiconductor device fabrication

Cite as: AIP Advances 13, 065113 (2023); doi: 10.1063/5.0144639
Submitted: 3 May 2023 • Accepted: 26 May 2023 •
Published Online: 9 June 2023

A. Wratten,[1] D. Walker,[2] E. Khorani,[1] B. F. M. Healy,[1] N. E. Grant,[1] and J. D. Murphy[1,a)]

AFFILIATIONS

[1] School of Engineering, University of Warwick, Coventry CV4 7AL, United Kingdom
[2] Department of Physics, University of Warwick, Coventry CV4 7AL, United Kingdom

[a)] Author to whom correspondence should be addressed: john.d.murphy@warwick.ac.uk

ABSTRACT

Thin film dielectrics are ubiquitous in the manufacture of electronic devices and are frequently deposited and etched away at various stages of device fabrication. We demonstrate that hafnium oxide (HfO_2) thin films grown via atomic layer deposition on silicon and silicon pre-coated with aluminum oxide (Al_2O_3) have etch resistance properties, which can be tuned simply by changing the post-deposition annealing temperature. The etching rates of films in hydrofluoric acid (HF) solutions were found to be dependent on annealing temperature, with the etch rate decreasing with increasing temperature. A transition region in the etch rate was identified between 300 and 350 °C, corresponding to the crystallization of the HfO_2 films, as identified via x-ray diffraction. HfO_2 films deposited directly onto silicon annealed above 350 °C were resistant to 10% HF solutions over the course of several hours. In the case of $Si/Al_2O_3/HfO_2$ stacks, closer inspection reveals the existence of channels, which reduces the etch resistance of HF acid, as evidenced by tetramethylammonium hydroxide etching of the silicon substrate. Crystallized HfO_2 can be used to protect other dielectrics in device processing, and we demonstrate its use in single-sided fabrication of patterned structures of Al_2O_3, which can control the effective charge-carrier lifetime in silicon wafers for use in modulating THz and mm-wave radiation.

I. INTRODUCTION

The manufacturing of semiconductor devices often requires the deposition and selective removal of thin-film dielectric layers. As such, it is vital to have a portfolio of dielectrics available with different etch resistances. Hafnium oxide (HfO_2) is a versatile material with applications in areas ranging from the high-temperature extreme environments of refractory ceramics[1] to sensitive structures for microelectronics.[2] As a high-*k* dielectric,[3] it has been well established that HfO_2 is capable of enhancing the performance of transistors[4] and capacitors[5] and, beyond this, has been found to have useful anti-reflective[6] and surface passivating properties.[7,8] Interestingly, HfO_2 is also remarkably robust, having demonstrated resistance to oxidation,[1] copper corrosion,[9] and general weathering.[10] Understanding and controlling the robustness of HfO_2 would enable the utilization of these films as protective barrier layers in semiconductor processing. It may also be possible to create smooth and uniform ultrathin (~1 nm) films by etching back thicker films without incurring the surface roughness and nucleation defect issues,[11] which occur in the direct growth of films at the single nanometer scale.

In this paper, we have determined the conditions under which HfO_2 grown by atomic layer deposition (ALD) has etch resistance. ALD is a low temperature process that allows for precise control and conformality of thin films.[12–14] The potential for low thermal budget depositions, combined with the compatibility with existing industrial processes, makes ALD an attractive approach for thin film deposition. ALD systems can also be used for the selective removal of thin films, known as atomic layer etching (ALE). ALE allows for fine control over etching rates but has the potential to result in surface damage, as with the case of plasma-etching,[15] or requires a higher temperature operating window, as with thermal-ALE.[16] As such,

we have instead focused on investigating the wet chemical etching behavior of HfO_2 films, as a less destructive, lower temperature alternative. Utilizing plasma-enhanced ALD and low/room temperature wet chemical etching could provide a low-thermal budget approach to ultrathin film growth.

The primary aim of this paper is to demonstrate the capabilities of HfO_2 as a controllable protective layer for electronic and photovoltaic device processing. As such, we have studied several solutions commonly used in silicon processing as potential etchants. This includes standard clean 1 (SC1 or RCA1 where "RCA" stands for Radio Corporation of America), standard clean 2 (SC2 or RCA2), tetramethylammonium hydroxide (TMAH), and hydrofluoric acid (HF). Where previous studies have focused solely on HfO_2 layers deposited directly onto silicon,[17–21] we have also investigated the etch resistance of HfO_2 that has been incorporated into $Si/Al_2O_3/HfO_2$ stacks. It is important to establish whether, in addition to protecting silicon, HfO_2 is also able to protect other sensitive dielectrics. This diversifies the ways in which HfO_2 protective layers may be incorporated into complex electronic device structures.

The results of this investigation have already proven useful in the development of devices for the modulation of THz and mm-wave radiation. HfO_2 films have been utilized to protect passivating Al_2O_3 layers on the rear of samples as they undergo patterning processes necessary for modulation.[22] We complete the paper by providing this as a case study for the use of HfO_2's etch resistance.

II. EXPERMENTAL METHODS

Si/HfO_2 and $Si/Al_2O_3/HfO_2$ stacked layers were deposited onto mirror polished silicon (100) wafers, cut to 5 × 5 cm^2 squares, via plasma-enhanced atomic layer deposition (PE-ALD) using a Veeco Fiji G2 system. Before deposition, the silicon wafers were cleaned using established processes,[23] starting with immersion in an RCA1 solution, consisting of de-ionized (DI) H_2O, NH_4OH (30%), and H_2O_2 (30%) in a 5:1:1 ratio. This was then followed by an RCA2 solution: DI H_2O, HCl (37%), and H_2O_2 (30%) in a 5:1:1 ratio. Both solutions were heated to ~80 °C, with H_2O_2 only added immediately before sample immersion. The samples spent 10 min in each solution, preceded by a DI water rinse and a 60 s 1% HF dip each time. The clean was completed with a final DI water rinse and 2% HF dip. Each sample was individually dipped until it could be pulled dry from the HF solution and was then immediately transferred to the ALD stage.

Depositions were performed at 200 °C, using O_2 plasma as the co-reactant and argon as the inert carrier gas. To produce HfO_2 films, a tetrakis(dimethylamido)hafnium (TDMAH) precursor was pulsed for 0.25 s, followed by 6 s of O_2 plasma at 300 W, with a 5 s purge step before and after each. Al_2O_3 films were produced by pulsing a trimethylaluminium (TMA) precursor for 0.06 s and O_2 plasma for 6 s at 300 W, purging for 4 s between each step. For single layer samples, 200 process cycles of HfO_2 were deposited on each side of the wafer. This was preceded by 160 cycles of Al_2O_3 for the $Si/Al_2O_3/HfO_2$ samples. Samples were then either left in their as-deposited state or annealed in air for 30 min using a quartz tube furnace at temperatures ranging from 250 to 400 °C.

The etch resistance of the single and stacked samples was investigated through measurement of HfO_2 film thickness, using a Filmetrics F40 reflectometry tool. Point measurements were taken at five different locations on a sample, and the results were averaged. The initial HfO_2 and Al_2O_3 film thicknesses were ~26 ± 3 and 21 ± 3 nm, respectively. It should be considered that the mathematical model implemented in the Filmetrics system assumes a constant density; it is therefore possible that measurement variations attributed to film thickness may also be influenced by changes in film density or surface roughness. However, the close fit of the Filmetrics model indicates that any such contributions are likely minimal. Samples were then submersed in one of the following solutions: RCA1, RCA2, 25% TMAH, or 10% HF. These are all solutions commonly used in the processing of silicon wafers. The RCA solutions were prepared as described for the initial cleaning process, the TMAH solution was heated to 80 °C, and the HF solution was kept at room temperature. At regular intervals, the samples would be removed from the solution and rinsed with DI water to pause the etching process, and the film thickness was measured.

Film crystallinity was investigated with grazing incidence x-ray diffraction (GI-XRD), using a third generation Malvern Panalytical Empyrean XRD diffractometer, equipped with a Pixcel3D detector and multicore (iCore, iCore) optics providing Cu $K\alpha_{1/2}$ radiation. The sample surface was aligned to the direct beam to ensure that it was at the center of rotation of the goniometer, and the incident angle was set to 0.5°. 2θ measurements were made in the range of 15°–70° 2θ. The data were fitted using the Malvern Panalytical HighScore Plus data analysis software.

Atomic force microscopy (AFM) was performed on certain etched samples using a Bruker Dimension Icon microscope in PeakForce Tapping Mode, with a ScanAsyst-Air tip.[24] The resulting images were processed using Gwyddion 2.60.

To demonstrate the utility of HfO_2 in device processing, we provide a case study of patterned surface passivation. In this part of the work, photolithography was performed using a custom-made photomask. The mask consisted of nine distinct 2.5 × 2.5 cm^2 regions, with different filling fractions of periodic square holes. An S1818 photoresist was spin-coated at 5000 rpm for 30 s, followed by a soft bake at 115 °C for 1 min. The photoresist was then exposed for 3 s (equivalent to a dose of ~130 mJ/cm^2) in soft contact mode with 100 μm mask-wafer separation, using a Suss MicroTec BA8 Gen3 mask aligner. Following exposure, the photoresist was developed in an MF319 solution for 45 s, followed by a rinse in DI water. To protect the photoresist during wet chemical etching, a hard bake at 130 °C for 5 min was conducted following development. The resulting structure was then etched in a 2% TMAH solution at room temperature for 25 min. Photoluminescence images were taken using a BT Imaging iLS-L1, with an exposure of 1 Sun (~1000 W m^{-2}) for 5 s.

III. RESULTS AND DISCUSSION

A. Wet chemical etching behavior

We first investigate the wet chemical etch resistance of HfO_2 films deposited directly onto silicon wafers (referred to as Si/HfO_2), whereby samples kept in their as-deposited state (at 200 °C) are compared to samples annealed at 400 °C in air for 30 min. Figure 1 shows how the film thickness of HfO_2, as measured via reflectometry, varies with time spent in each of the solutions. As seen in Figs. 1(a)–1(c), excellent resistance is demonstrated for samples

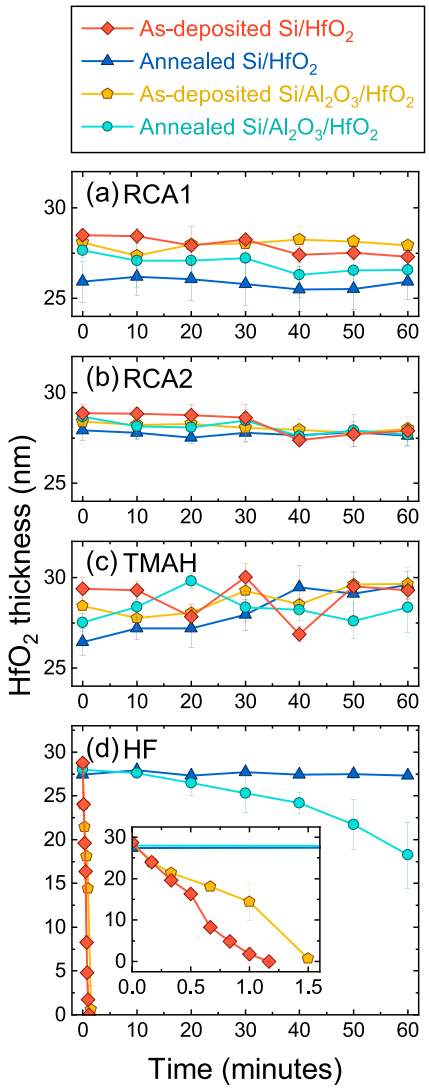

FIG. 1. Thickness of HfO_2 films deposited on silicon and Al_2O_3 on silicon, measured via reflectometry, as a function of time spent in an (a) RCA1, (b) RCA2, (c) TMAH (25%), or (d) HF (10%) solution. The inset in (d) shows the first 1.5 min of etching. As-deposited Si/HfO_2 (red diamonds) and $Si/Al_2O_3/HfO_2$ films (yellow pentagons) are compared to samples annealed at 400 °C for 30 min in air (dark blue triangles and light blue circles for single layers and stacks, respectively).

in RCA1, RCA2, and TMAH solutions, with no change in film thickness observed after 1 h for both as-deposited and annealed samples. Remarkably, annealed Si/HfO_2 layers also show no change in film thickness, even after 1 h in a 10% HF solution [Fig. 1(d)]. This outperforms both SiO_2, which has an etch rate of 1 nm/s with the same HF concentration,[25] and Al_2O_3, which has an etch rate of 0.8 nm/s in only 1% HF.[26] For a wet chemical etching approach for the creation of ultrathin crystalline HfO_2 films to be viable, the use of higher concentrations of HF could be considered. However, rapid etching is seen in the as-deposited sample, as can be seen in the inset of Fig. 1(d). This result is supported by the works of Murdzek and George[27] and Lowalekar and Raghavan,[20] who also noticed a significantly more rapid etch rate for as-deposited Si/HfO_2 samples than the ones that had been heat-treated. The fact that it is possible to control the chemical etch resistance with a simple anneal treatment is investigated further later.

An intended application of this HfO_2 layer is to protect other dielectric layers from being etched, and the wet chemical etch resistance of $Si/Al_2O_3/HfO_2$ stacks was also studied. As such, Fig. 1 also shows the variation in thickness of HfO_2 films, deposited on Al_2O_3, during immersion in RCA1, RCA2, TMAH, or HF solutions. In the first three solutions [Figs. 1(a)–1(c)], stacked samples show a similar response to single layer HfO_2 films, in both the as-deposited and annealed cases. This would indicate that the integrity of the HfO_2 etch resistance to these solutions is not influenced by a layer beneath. Looking at the etch resistance to HF in Fig. 1(d), we again see similar etch rates between as-deposited single layer and stacked samples, with rapid, linear etching in under 2 min. However, it is apparent that, once annealed, the inclusion of an Al_2O_3 layer reduces the etch resistance of the HfO_2 film to HF, with the $Si/Al_2O_3/HfO_2$ etching slowly over the course of several hours. The etching of the annealed $Si/Al_2O_3/HfO_2$ sample is much slower, less linear, and less uniform than in the as-deposited case, indicating that a different etching mechanism is responsible. It should be noted that, although reduced, the stacked sample still demonstrates a substantially increased etch resistance compared to an Al_2O_3 layer alone and thus would provide sufficient protection in most chemical processing scenarios.

From Fig. 1, it is clear that a post-deposition annealing treatment substantially changes the wet chemical etching behavior of the single- and double-layer dielectric films. Therefore, to investigate this dependence further, we examine the etch resistance of Si/HfO_2 and $Si/Al_2O_3/HfO_2$ samples annealed at temperatures between 250–400 °C for 30 min. In Fig. 2 the results of this investigation, averaged across several repeated experiments, are plotted. For the Si/HfO_2 samples, Fig. 2(a) demonstrates that etching occurs on three different time scales. Samples annealed above 350 °C typically show no measurable sign of etching after 3 h in a 10% HF solution, while samples annealed below 300 °C etch rapidly, being fully removed within a few minutes. Between these two temperatures, there is a transition region, highlighted by the orange band, where samples etch slowly over the course of several hours. It is helpful to have such a transition region in the wet chemical etch resistance of HfO_2 films. Etching of films annealed within this temperature region may provide a route to high-quality, non-amorphous, ultrathin HfO_2 layers, without the need for higher concentrations of HF.

Figure 2(b) shows the annealing temperature dependence of the etch resistance of stacked $Si/Al_2O_3/HfO_2$ samples to HF. We can again identify a low-temperature region, where films etch rapidly, and a transition region, between 300 and 350 °C, where films etch more slowly, similar to the single layer HfO_2 films shown in Fig. 2(a). However, looking at the high-temperature region (above 350 °C), we now see very slow etching of the stacked samples, as highlighted by the orange band. At annealing temperatures of ≥350 °C, where the single layer HfO_2 films showed complete resistance to etching, the corresponding Al_2O_3/HfO_2 stacked layers in Fig. 2(b) do not. From this, we infer that the dependence of the underlayer on the etch

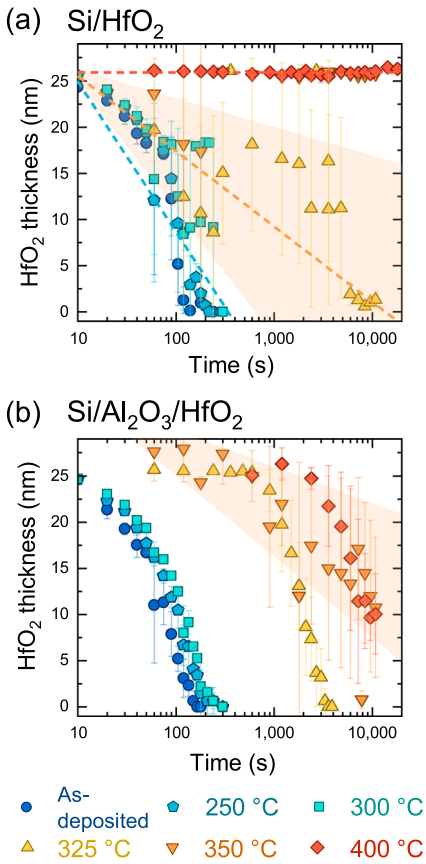

FIG. 2. Thickness of HfO_2 films deposited at 200 °C on (a) silicon and (b) 20 nm of Al_2O_3 on silicon annealed at different temperatures, measured via reflectometry, as a function of time spent in a 10% HF solution. This dataset is produced from averaging results across up to six repeated experiments. The orange shaded bands are discussed in the main text.

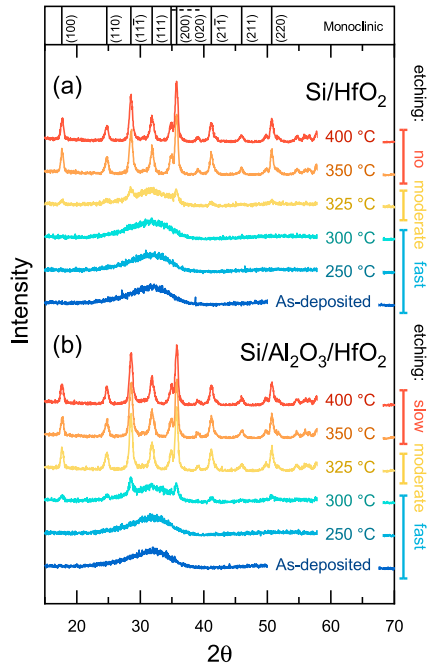

FIG. 3. GI-XRD patterns, using a Cu K-α source, taken from samples of 26 nm (200 cycles) of HfO_2 deposited (a) directly onto polished silicon and (b) on polished silicon samples with a 20 nm (160 cycles) Al_2O_3 interlayer. Samples were annealed in air for 30 min at temperatures ranging from as-deposited (200 °C) to 400 °C. Patterns have been offset for clarity, and the main crystallographic planes are indexed at the top. The different regimes of etching in HF are labeled on the right.

resistance (in HF solutions) only becomes apparent once annealed ≥350 °C.

B. HfO_2 film crystallinity

To investigate any potential correlation between the etch resistance of the single or stacked samples and the crystallinity of the HfO_2 layer, we apply GI-XRD to samples that are annealed between 250–400 °C, with the patterns presented in Fig. 3. From Fig. 3(a), we have identified that 26 nm thick HfO_2 films on silicon crystallize between 300 and 350 °C. Below this temperature range, the HfO_2 films are primarily in an amorphous state, while above 350 °C, we see clear peaks that correspond to a distinct crystal structure. These peaks have been indexed according to a monoclinic HfO_2 crystal structure.[28]

The variation in crystal structure with annealing temperature corresponds closely to the three stages of HF etch resistance we observed in Fig. 2, with amorphous samples etching quickly, crystallized samples showing no evidence of etching, and samples around the crystallization region etching at an intermediate time scale. In contrast, however, we see no notable distinction in the crystal structure of HfO_2 on Al_2O_3 compared to HfO_2 on silicon, as shown in Fig. 3(b). Thus, the etch resistance of the 400 °C annealed stacked samples is not related to differences in the crystallized structure of the HfO_2 layer.

C. Etching mechanisms

To investigate potential causes for variations in etching rates, it was first necessary to ensure that this difference in behavior was not a matter of physical damage to the samples that could occur during handling. To examine this, we conducted a scratch test, where a sample of each type was scratched diagonally from corner to corner and placed alongside unscratched samples in an HF solution. The result of this investigation can be seen in Fig. 4, which also includes a schematic of the scratch and approximate measurement points. Measurements were taken at varying distances from the scratch but not directly over it. It is apparent that this degree of physical damage has no influence upon the etching behavior of either the single layer Si/HfO_2 or the stacked $Si/Al_2O_3/HfO_2$ films. This demonstrates that the protective capabilities of HfO_2 are remarkably unimpeded by physical damage. It also implies that there must be other mechanisms responsible for the reduced etch resistance of high temperature stacked samples.

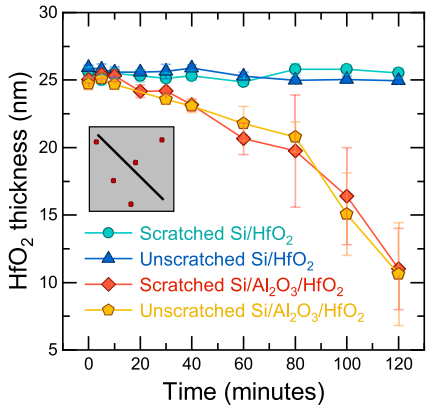

FIG. 4. Thickness of HfO_2 films, deposited on top of either a 20 nm thick Al_2O_3 layer or directly onto silicon, annealed at 400 °C in air for 30 min, as a function of time in a 10% HF solution. Samples scratched with a diamond scribe are compared to unscratched samples. A diagram of the method of scratching, and measurement locations, is shown within the figure.

We next consider the possibility that the etching solutions are, in some way, traveling through the overlaying films to the underlying substrate. It has been well established that TMAH etching solutions create distinct square-based pyramid etch pits in Si(100).[29,30] We compared Si/HfO_2 and $Si/Al_2O_3/HfO_2$ samples in their as-deposited and annealed states after 1 h in a 25% TMAH solution at 80 °C. In the case of single layer Si/HfO_2 samples, we see no evidence of TMAH etching under an optical microscope; this is also the case for the as-deposited stacked samples. However, once annealed, the stacked sample shows extensive etching of the underlying silicon substrate across the entire sample, despite having already established there is no change in the measured film thickness.

A close-up optical microscope image of the annealed and TMAH-etched stacked sample can be seen in Fig. 5(a), which clearly shows the distinct square shape of the etch pits. This implies that the annealing of $Si/HfO_2/Al_2O_3$ stacked samples creates channels throughout the entire structure, through which the TMAH can pass through to the underlying silicon, as depicted in Fig. 5(b).

Through application of AFM, we have imaged the shape of these channels after the etching process. An image of a single etch pit, as well as the corresponding depth profile, can be seen in Figs. 5(c) and 5(d). Note that the dimensions of the AFM tip prevent measurement of the full depth of the etch pit, with the value obtained here cutting off at around −0.8 μm. These results would suggest that the dielectrics directly over the etch pits become undermined and are thus removed by the solution, leaving a channel through the entire structure that is the size and shape of the etch pit below. The initial form of these channels before etching has not yet been identified, although there is the potential for them to take the form of pinholes. If controlled, pinholes can behave as a beneficial charge carrier transport mechanism, acting as an alternative tunneling process through thin film structures. In particular, this may prove useful in the field of photovoltaics, for applications in passivating contacts.[31] These channels do not appear to be present in the as-deposited case or in the single layer Si/HfO_2 samples.

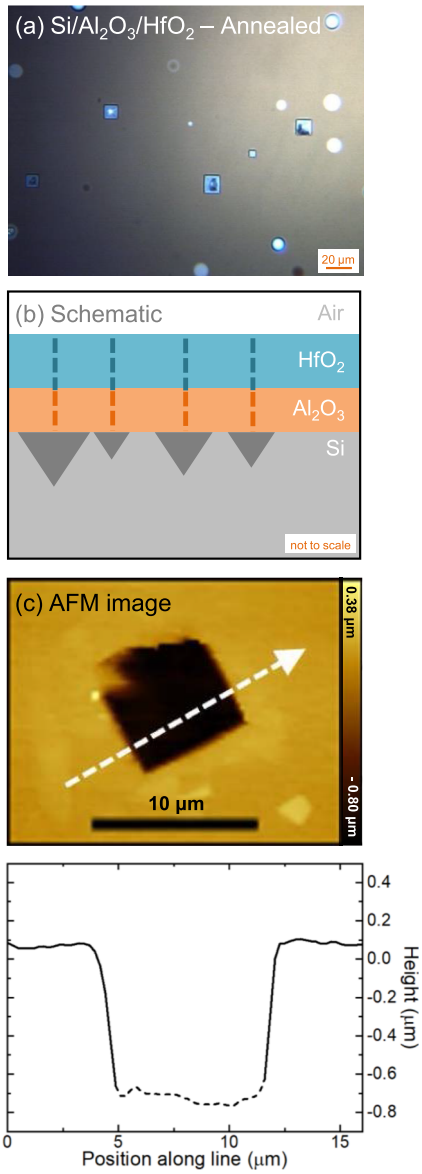

FIG. 5. (a) Optical microscope image of a stacked $Si/Al_2O_3/HfO_2$ sample, annealed at 400 °C, after 1 h in a 25% TMAH solution at 80 °C. (b) An illustration of the etch pits apparent in the structure, with the dashed lines representing some form of channel through the structure. (c) An AFM scan of a single etch pit in the annealed $Si/Al_2O_3/HfO_2$ sample. (d) The depth profile of the etch pit in (c), with the data collected along the white arrow. The dashed section in (d) does not correspond to the physical profile of the base of the etch pit and results from limitations of the AFM tip dimensions.

The same behavior can be seen in annealed stacked samples during immersion in HF, as depicted in Fig. 6. Visible channels appear in the stacked structure after around 20 min, which then expand over time. This is likely due to the HF passing through channels in the HfO_2 layer to the Al_2O_3 layer beneath, which will then etch more quickly locally. HfO_2 is eventually undermined and will

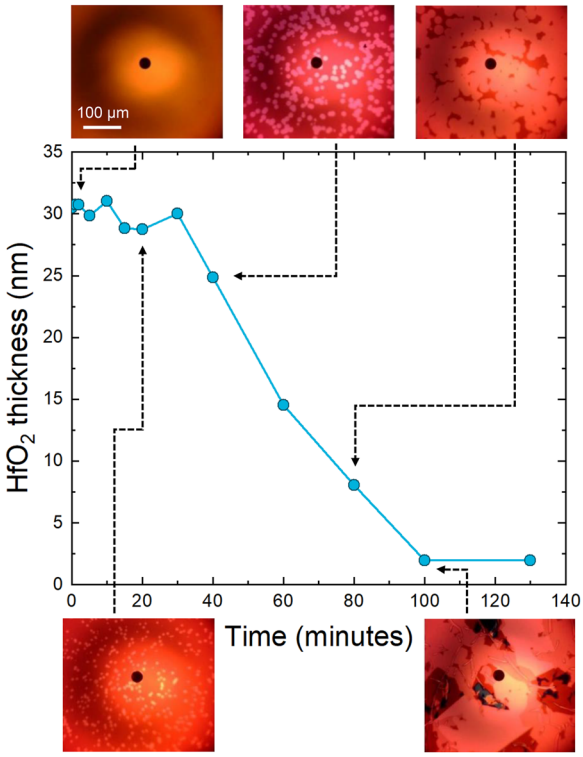

FIG. 6. Thickness measurements and optical micrographs of a specific region on a stacked $Si/Al_2O_3/HfO_2$ sample, annealed at 350 °C, during immersion in 10% HF. Each micrograph corresponds to a specific data point on the thickness plot. The black dots on each image highlight the reflectometry measurement point.

delaminate, as can be seen in the final micrograph. This apparent channel structure may be responsible for the change in the etching behavior that we see in annealed stacked samples, compared to the other sample variations that have been investigated. However, it is not yet clear why these channels are not present in either single layer Si/HfO_2 samples or as-deposited stacked $Si/Al_2O_3/HfO_2$ samples. A possible explanation would be the diffusion of hydrogen, or other elements, through the layers in the sample that occurs during the post-deposition annealing stage. Blistering, resulting from high temperature annealing, may also be a potential factor.[32,33]

D. Using the etch resistance of HfO_2 films in the fabrication of patterned structures

The benefits of the etch resistance of HfO_2 films are shown in the following example of a fabrication process used to produce a patterned passivation layer to control the carrier lifetime in semiconductor devices. Such lifetime control is needed in the fabrication of mm-wave or THz modulation devices. Such devices are particularly useful for quality-control and security imaging purposes, enabling for non-invasive screening of stacked or concealed materials, such as dielectrics, plastics, and textiles.[34]

To achieve a suitable trade-off between modulation and switching speed in THz photomodulators, it is necessary to control the effective lifetime in the device.[35] The carrier lifetime level required often lies in between the value required by two well passivated surfaces and a completely unpassivated wafer. One way of achieving such an intermediate lifetime is to pattern the surface passivation on one side, which was the approach used in a recent study by Hooper *et al.*[22] The production of such a photomodulator was enabled by the use of an etch-resistant HfO_2 layer on the rear, as described in this current paper.

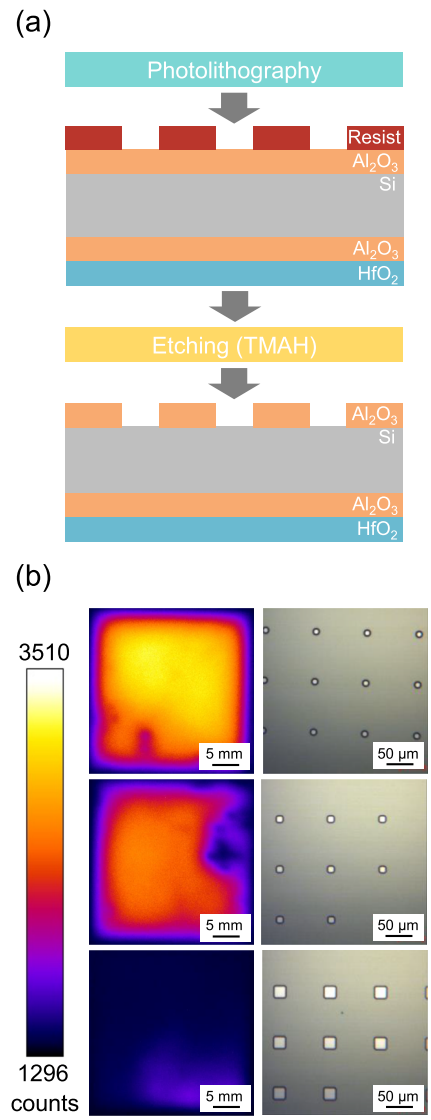

FIG. 7. (a) Process sequence involving the use of a rear HfO_2 protective layer to fabricate a patterned front-side passivated THz photomodulator. The HfO_2 layer provides protection against etching for the rear Al_2O_3 passivation, while the front is patterned and etched through a combination of photolithography and immersion into a 2% TMAH solution at room temperature for 25 min. (b) Photoluminescence images acquired with the same exposure conditions (1 Sun, 5 s) of samples with different filling factors on the front Al_2O_3 surface, producing samples with tunable carrier lifetimes. The optical micrographs show patterned passivation structures, with Al_2O_3 having been removed from the lighter-colored periodic features.

A schematic of the fabrication process can be seen in Fig. 7(a). Both sides of a high lifetime silicon wafer were passivated by Al_2O_3 films. A HfO_2 layer is then deposited over the Al_2O_3 on the rear. The sample is then annealed at 450 °C, with the temperature required for optimal Al_2O_3 passivation being above the crystallization temperature of the HfO_2 layer. The crystallized HfO_2 becomes strongly resistant to wet chemical etching, in comparison to the exposed Al_2O_3 layer on the front. Photolithography is then used to pattern the front Al_2O_3 layer, and immersion into a 2% TMAH solution results in etching of the front Al_2O_3 according to the photolithography pattern, while the rear Al_2O_3 is protected by the HfO_2.

Importantly, stacking the Al_2O_3 and HfO_2 does not result in any substantial decline in passivation quality. Consistent and high-quality passivation is essential so that the carrier lifetime of each device can then be carefully controlled through the patterning process on the front side. Each pattern has a different filling fraction, with an increased filling fraction indicating the increasing size of holes within the passivation layer, corresponding to a decrease in carrier lifetime. Examples of samples with patterns of increasing filling fraction, and thus decreasing passivation, can be seen in Fig. 7(b). This example illustrates the potential of using HfO_2 protective films in the fabrication of semiconductor devices.

IV. CONCLUSION

We have studied the etch resistance of single layer Si/HfO_2 and stacked $Si/Al_2O_3/HfO_2$ structures to solutions commonly used in silicon processing. HfO_2 deposited directly onto Si has been demonstrated to have excellent etch resistance to RCA1, RCA2, and TMAH, showing no indication of variation in film thickness after 1 h in each solution. Si/HfO_2 samples annealed above 350 °C also show no sign of etching after 1 h in a 10% HF solution, although etch rates increase dramatically with lower temperature annealing. A correlation between the etch rates of HfO_2 films in HF with the HfO_2 film crystallinity was identified, with amorphous films annealed <300 °C etching quickly, crystallized films annealed >350 °C not etching within the timeframe, and a transition period being observed between these temperatures where the film begins to crystallize.

In the case of annealed $Si/Al_2O_3/HfO_2$ stacked samples, a reduction in etch resistance was identified, compared to the single layer counterparts. We have established that this reduced etch resistance is not a consequence of changes in the HfO_2 crystallized structure and is not likely to be related to handling damage of the samples. By investigating the TMAH etching of stacked samples, we have found evidence for channels within the annealed $Si/Al_2O_3/HfO_2$ structure, which allow chemical solutions to penetrate down to the silicon below. In the case of TMAH, the HfO_2 and Al_2O_3 films themselves are not etched as there is no change in the measured film thickness. However, in a 10% HF solution, the Al_2O_3 layer beneath the HfO_2 does seem to etch away, resulting in undermining and delamination of the HfO_2 film. Different interlayers may influence chemical etch resistance, as with the $Si/Al_2O_3/HfO_2$ stack, due to the formation of channels within the sample structure.

The excellent etch resistance of HfO_2 films, as demonstrated in this study, suggests a promising potential for applications as protective barrier layers in silicon-based electronic and photovoltaic device structures. The use of HfO_2 thin films as a protective barrier has already proved useful in the research of THz and mm-wave modulation and has the potential to be applied to a variety of different stacked structures. This work will become even more important as device structures and silicon processing techniques continue to develop in complexity.

ACKNOWLEDGMENTS

A.W. acknowledges the funding from the Engineering and Physical Sciences Research Council Doctoral Training Partnership (Grant No. EP/R513374/1). This work has been partially supported by EPSRC grants (Grant Nos. EP/S036261/1 and EP/V037749/1). The PL imaging setup was funded by an EPSRC First Grant (Grant No. EP/J01768X/2). XRD measurements were made using equipment housed within the X-ray Diffraction Research Technology Platform at Warwick. D.W. acknowledges the funding through EPSRC Grant No. EP/V007688/1.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

A. Wratten: Conceptualization (equal); Formal analysis (equal); Investigation (lead); Methodology (lead); Validation (lead); Visualization (lead); Writing – original draft (lead). **D. Walker**: Formal analysis (equal); Resources (supporting); Writing – review & editing (supporting). **E. Khorani**: Investigation (supporting); Writing – review & editing (supporting). **B. F. M. Healy**: Investigation (supporting); Writing – review & editing (supporting). **N. E. Grant**: Conceptualization (equal); Supervision (equal); Writing – review & editing (supporting). **J. D. Murphy**: Conceptualization (equal); Funding acquisition (lead); Project administration (lead); Resources (lead); Supervision (equal); Writing – review & editing (lead).

DATA AVAILABILITY

Data underpinning the figures in this paper can be downloaded from https://wrap.warwick.ac.uk/176080/. Requests for additional data should be made directly to the corresponding author. For the purpose of open access, the author has applied a Creative Commons Attribution (CC BY) license to any author-accepted manuscript version arising from this submission.

REFERENCES

[1] K. Mergia, V. Liedtke, T. Speliotis, G. Apostolopoulos, and S. Messoloras, "Thermo-mechanical behaviour of HfO_2 coatings for aerospace applications," Adv. Mater. Res. **59**, 87–91 (2008).

[2] J. H. Choi, Y. Mao, and J. P. Chang, "Development of hafnium based high-*k* materials—A review," Mater. Sci. Eng.: R: Rep. **72**, 97–136 (2011).

[3] V. A. Gritsenko, T. V. Perevalov, and D. R. Islamov, "Electronic properties of hafnium oxide: A contribution from defects and traps," Phys. Rep. **613**, 1–20 (2015).

[4]H. Mulaosmanovic, E. T. Breyer, S. Dünkel, S. Beyer, T. Mikolajick, and S. Slesazeck, "Ferroelectric field-effect transistors based on HfO_2: A review," Nanotechnology **32**, 502002 (2021).
[5]M. Pešić, F. Fengler, L. Larcher, A. Padovani, T. Schenk, E. D. Grimley, X. Sang, J. M. LeBeau, S. Slesazeck, U. Schroeder, and T. Mikolajick, "Physical mechanisms behind the field-cycling behaviour of HfO_2-based ferroelectric capacitors," Adv. Funct. Mater. **26**, 4601–4612 (2016).
[6]J. M. Khoshman, A. Khan, and M. E. Kordesch, "Amorphous hafnium oxide thin films for antireflection optical coatings," Surf. Coat. Technol. **202**, 2500–2502 (2008).
[7]A. Wratten, S. L. Pain, D. Walker, A. B. Renz, E. Khorani, T. Niewelt, N. E. Grant, and J. D. Murphy, "Mechanisms of silicon surface passivation by negatively charged hafnium oxide thin films," IEEE J. Photovoltaics **13**, 40–47 (2023).
[8]S. L. Pain, E. Khorani, T. Niewelt, A. Wratten, G. J. Paez Fajardo, B. P. Winfield, R. S. Bonilla, M. Walker, L. F. J. Piper, N. E. Grant, and J. D. Murphy, "Electronic characteristics of ultra-thin passivation layers for silicon photovoltaics," Adv. Mater. Interfaces **9**, 2201339 (2022).
[9]J. S. Daubert, G. T. Hill, H. N. Gotsch, A. P. Gremaud, J. S. Ovental, P. S. Williams, C. J. Oldham, and G. N. Parsons, "Corrosion protection of copper using Al_2O_3, TiO_2, ZnO, HfO_2, and ZrO_2 atomic layer deposition," ACS Appl. Mater. Interfaces **9**, 4192–4201 (2017).
[10]M. Fadel, O. A. Azim M., O. A. Omer, and R. R. Basily, "A study of some optical properties of hafnium dioxide (HfO_2) thin films and their applications," Appl. Phys. A: Mater. Sci. Process. **66**, 335–343 (1998).
[11]S. M. George and Y. Lee, "Prospects for thermal atomic layer etching using sequential, self-limiting flourination and ligand-exchange reactions," ACS Nano **10**, 4889–4894 (2016).
[12]R. W. Johnson, A. Hultqvist, and S. F. Bent, "A brief review of atomic layer deposition: From fundamentals to applications," Mater. Today **17**, 236–246 (2014).
[13]H. C. M. Knoops, S. E. Potts, A. A. Bol, and W. M. M. Kessels, *Handbook of Crystal Growth*, 2nd ed. (Elsevier, 2015), pp. 1101–1134.
[14]R. L. Puurunen, "A short history of atomic layer deposition: Tuomo Suntola's atomic layer epitaxy," Chem. Vap. Deposition **20**, 332–344 (2014).
[15]K. J. Kanarik, T. Lill, E. A. Hudson, S. Sriraman, S. Tan, J. Marks, V. Vahedi, and R. A. Gottscho, "Overview of atomic layer etching in the semiconductor industry," J. Vac. Sci. Technol. **33**, 020802 (2015).
[16]A. Fischer, A. Routzahn, S. M. George, and T. Lill, "Thermal atomic layer etching: A review," J. Vac. Sci. Technol. **39**, 030801 (2021).
[17]C. T. Kuo, R. Kwor, and K. M. Jones, "Study of sputtered HfO_2 thin films on silicon," Thin Solid Films **213**, 257–264 (1992).
[18]J. Chen, W. J. Yoo, D. S. H. Chan, and D.-L. Kwong, "Effects of annealing and Ar ion bombardment on the removal of HfO_2 gate dielectric," Electrochem. Solid-State Lett. **7**, F18–F20 (2004).
[19]H. Grüger, C. Kunath, E. Kurth, S. Sorge, W. Pufe, and T. Pechstein, "High quality r.f. sputtered metal oxides (Ta_2O_5, HfO_2) and their properties after annealing," Thin Solid Films **447–448**, 509–515 (2004).
[20]V. Lowalekar and S. Raghavan, "Etching of zirconium oxide, hafnium oxide, and hafnium silicates in dilute hydrofluoric acid solutions," J. Mater. Res. **19**, 1149–1156 (2004).
[21]M. Seo, S. K. Kim, K.-M. Kim, T. Park, J. H. Kim, C. S. Hwang, and H. J. Cho, "Crystallization and wet etching characteristics of atomic layer deposited HfO_2 films using $Hf([N(CH_3)(C_2H_5)]_3[OC(CH_3)_3])$ precursor and O_3 oxidant," ECS Trans. **1**, 211–217 (2006).
[22]I. R. Hooper, E. Khorani, X. Romain, L. E. Barr, T. Niewelt, S. Saxena, A. Wratten, N. E. Grant, J. D. Murphy, and E. Hendry, "Engineering the carrier lifetime and switching speed in Si-based mm-wave photomodulators," J. Appl. Phys. **132**, 233102 (2023).
[23]N. E. Grant, T. Niewelt, N. R. Wilson, E. C. Wheeler-Jones, J. Bullock, M. Al-Amin, M. C. Schubert, A. C. Van Veen, A. Javey, and J. D. Murphy, "Superacid-treated silicon surfaces: Extending the limit of carrier lifetime for photovoltaic applications," IEEE J. Photovoltaics **7**, 1574–1583 (2017).
[24]K. Xu, W. Sun, Y. Shao, F. Wei, X. Zhang, W. Wang, and P. Li, "Recent development of PeakForce Tapping mode atomic force microscope and its applications on nanoscience," Nanotechnol. Rev. **7**, 605–621 (2018).
[25]G. A. C. M. Spierings, "Wet chemical etching of silicate glasses in hydrofluoric acid based solutions," J. Mater. Sci. **28**, 6261–6273 (1993).
[26]G. Masmitjà, P. Ortega, I. Martin, J. Pérez, G. López, E. Calle, L. G. Gerling, C. Voz, and R. Alcubilla, "Cost-effective cleaning solutions based on $H_2O/NH_3/H_2O_2$ mixtures for ALD Al_2O_3 passivated IBC c-Si solar cells," in *Spanish Conference on Electron Devices* (IEEE, 2017).
[27]J. A. Murdzek and S. M. George, "Thermal atomic layer etching of amorphous and crystalline hafnium oxide, zirconium oxide, and hafnium zirconium oxide," in *2019 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)* (IEEE, 2019).
[28]C. E. Curtis, L. M. Doney, and J. R. Johnson, "Some properties of hafnium oxide, hafnium silicate, calcium hafnate, and hafnium carbide," J. Am. Ceram. Soc. **37**, 458–465 (1954).
[29]L. M. Landsberger, S. Naseh, M. Kahrizi, and M. Paranjape, "On hillocks generated during anisotropic etching of Si in TMAH," J. Microelectromech. Syst. **5**, 106–116 (1996).
[30]P. Papet, O. Nichiporuk, A. Kaminski, Y. Rozier, J. Kraiem, J.-F. Lelievre, A. Chaumartin, A. Fave, and M. Lemiti, "Pyramidal texturing of silicon solar cells with TMAH chemical anisotropic etching," Sol. Energy Mater. Sol. Cells **90**, 2319–2328 (2006).
[31]K. Lancaster, S. Großer, F. Feldmann, V. Naumann, and C. Hagendorf, "Study of pinhole conductivity at passivated carrier-selected contacts of silicon solar cells," Energy Procedia **92**, 116–121 (2016).
[32]J. Kim, M. Ju, Y. Kim, and J. Yi, "Chemical stoichiometry effect of hafnium oxide (HfO_x) for passivation layer of PERC solar cells," Mater. Sci. Semicond. Process. **148**, 106833 (2022).
[33]D. Suh, "Etch characteristics and morphology of Al_2O_3/TiO_2 stacks for silicon surface passivation," Sustainability **11**, 3857 (2019).
[34]M. Rahm, J.-S. Li, and W. J. Padilla, "THz wave modulators: A brief review on different modulation techniques," J. Infrared, Millimeter, Terahertz Waves **34**, 1–27 (2012).
[35]I. R. Hooper, N. E. Grant, L. E. Barr, S. M. Hornett, J. D. Murphy, and E. Hendry, "High efficiency photomodulators for millimeter wave and THz radiation," Sci. Rep. **9**, 18304 (2019).