

3C-SiC on Si Lateral Power Devices

Technical Progress & Future Plan

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Introduction

Device theme



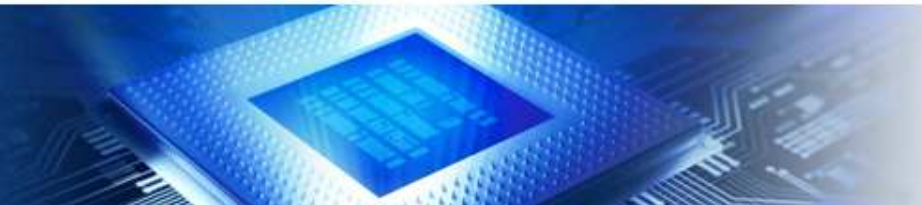
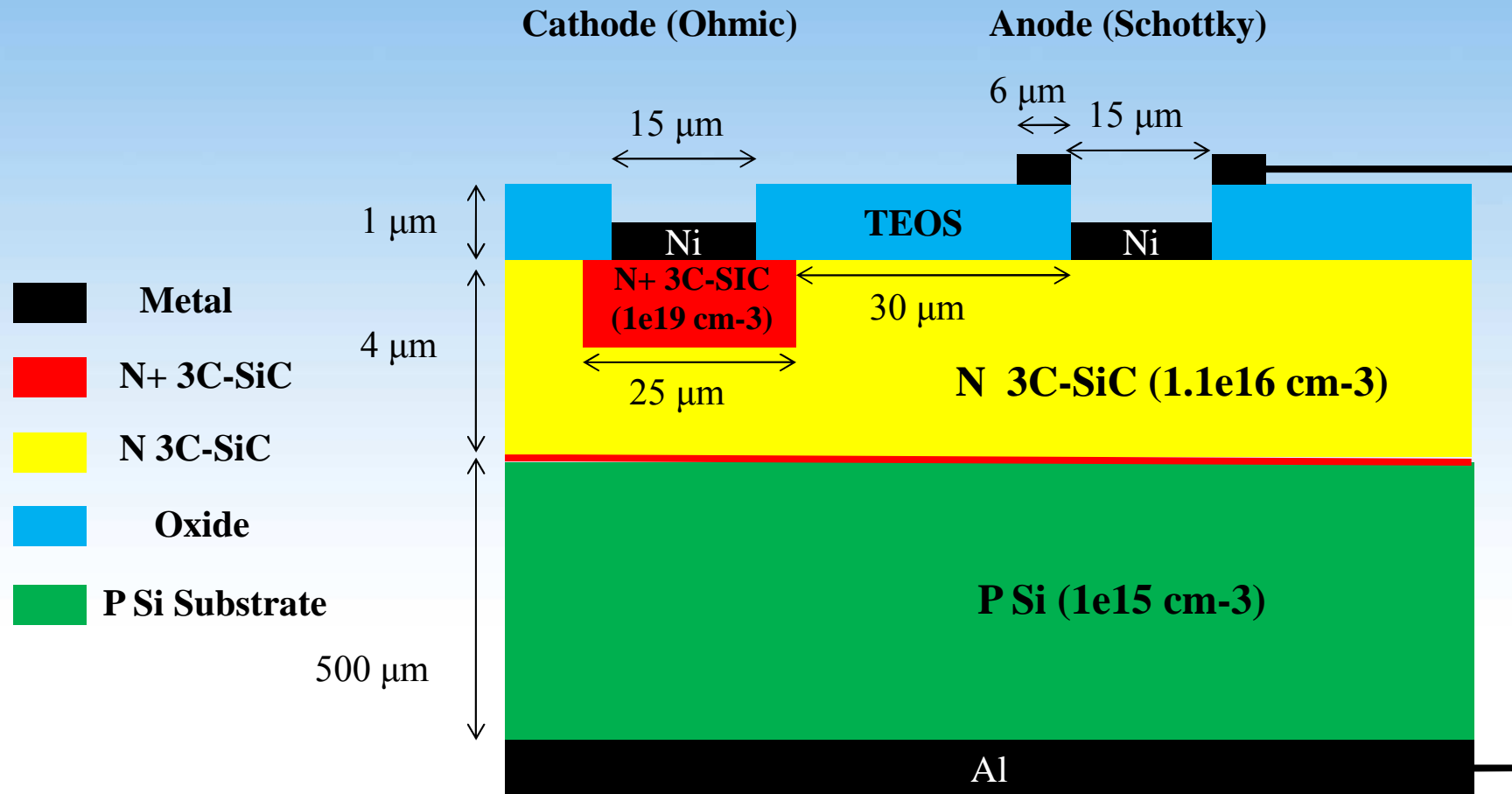
Lateral Schottky
diode



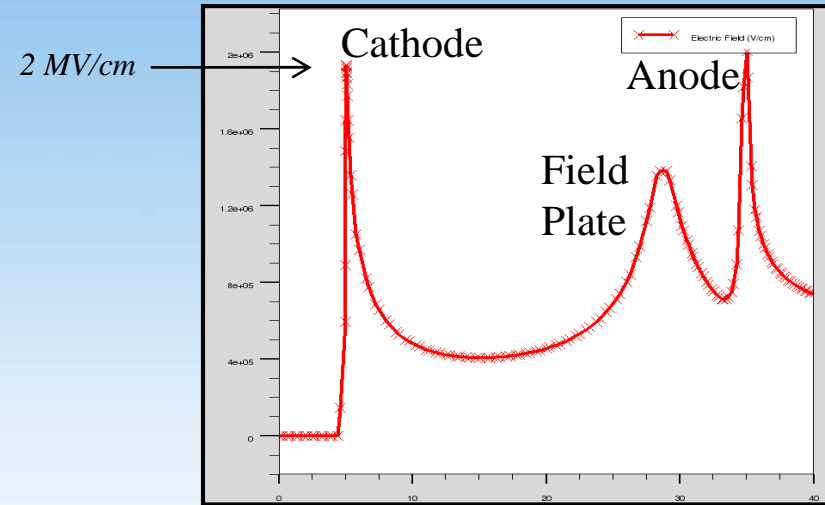
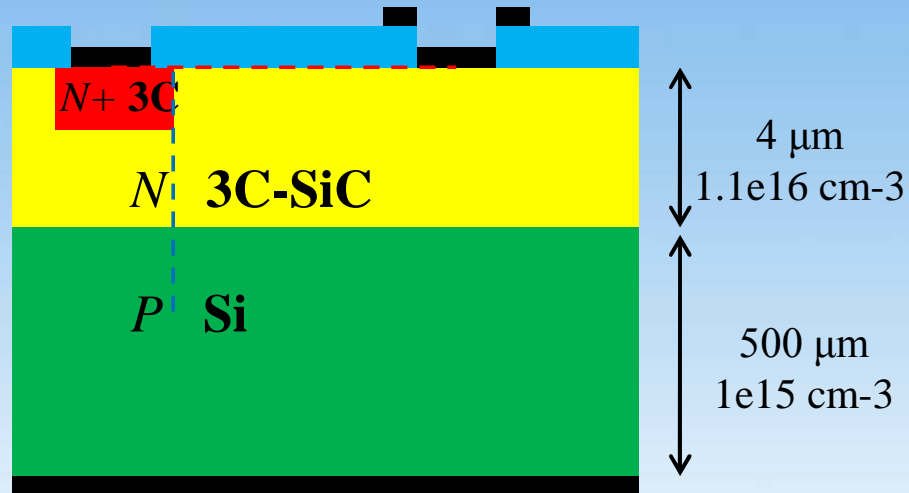
Lateral MOSFET



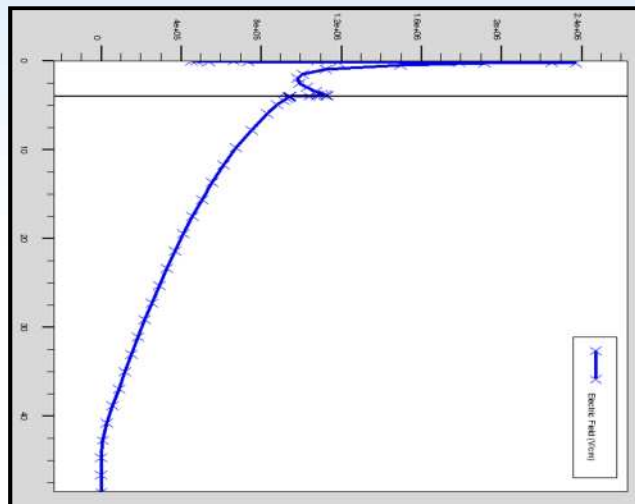
Lateral RESURF 3C-SiC SBD



2D Device Modelling



Lateral Electric Field at Contact Interface

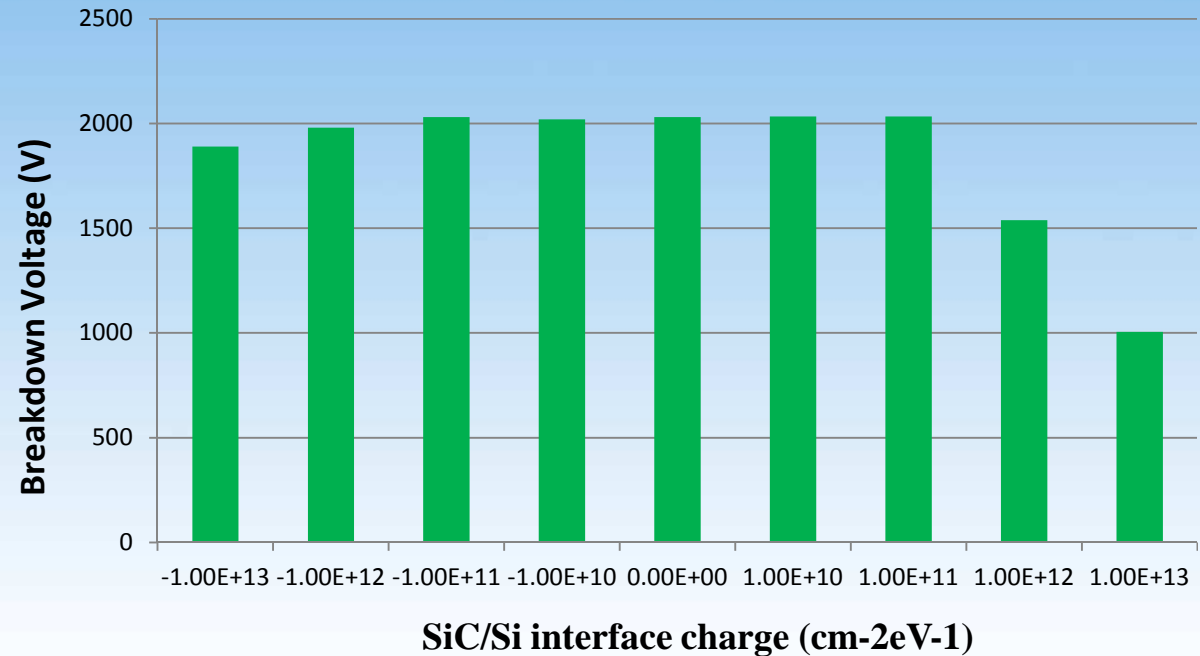
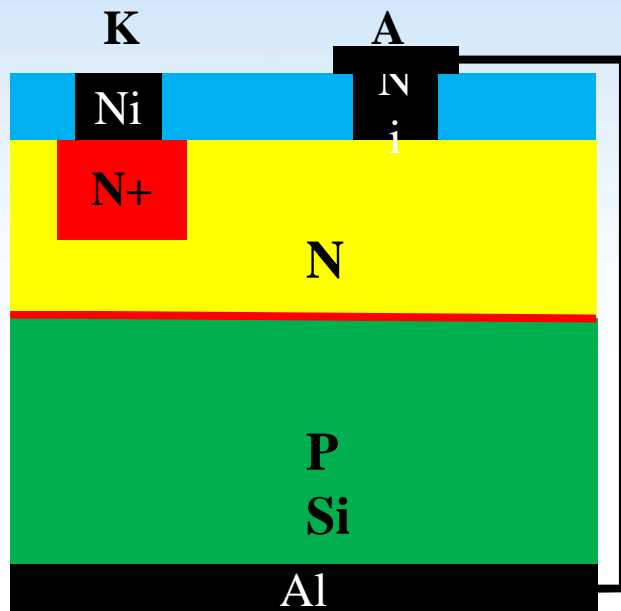


Vertical Electric Field

*2D simulation showed promising results:
breakdown voltage of 1870 V and forward
current density of 426 A/cm².*



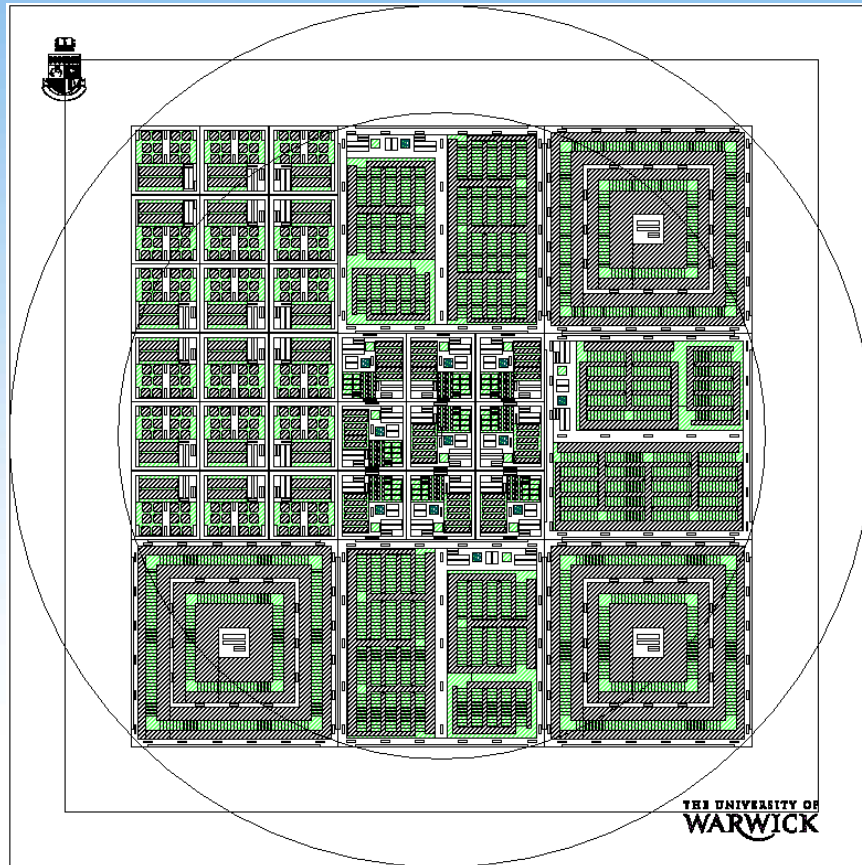
Charge at the SiC/Si interface



Positive charge at SiC/Si interface proved to be more influential in breakdown voltage

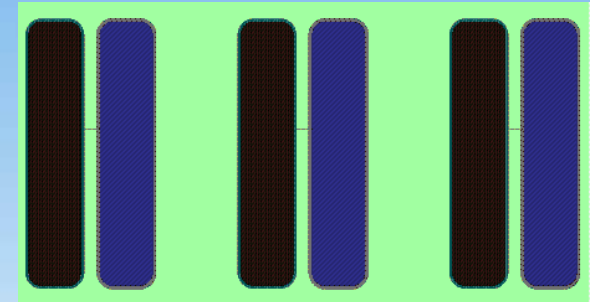


Mask Design for Lateral SBD

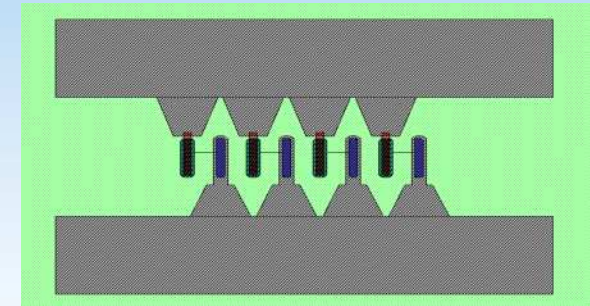


Mask design of the lateral Schottky diode, devices rated in orders of 10mA to more than 10 A are included.

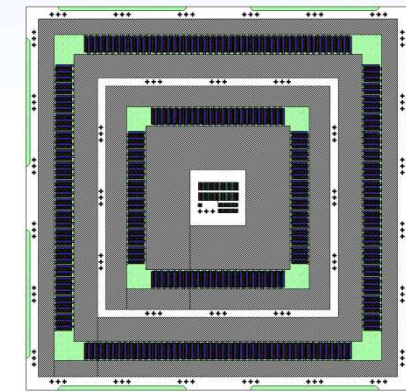
Single Cells



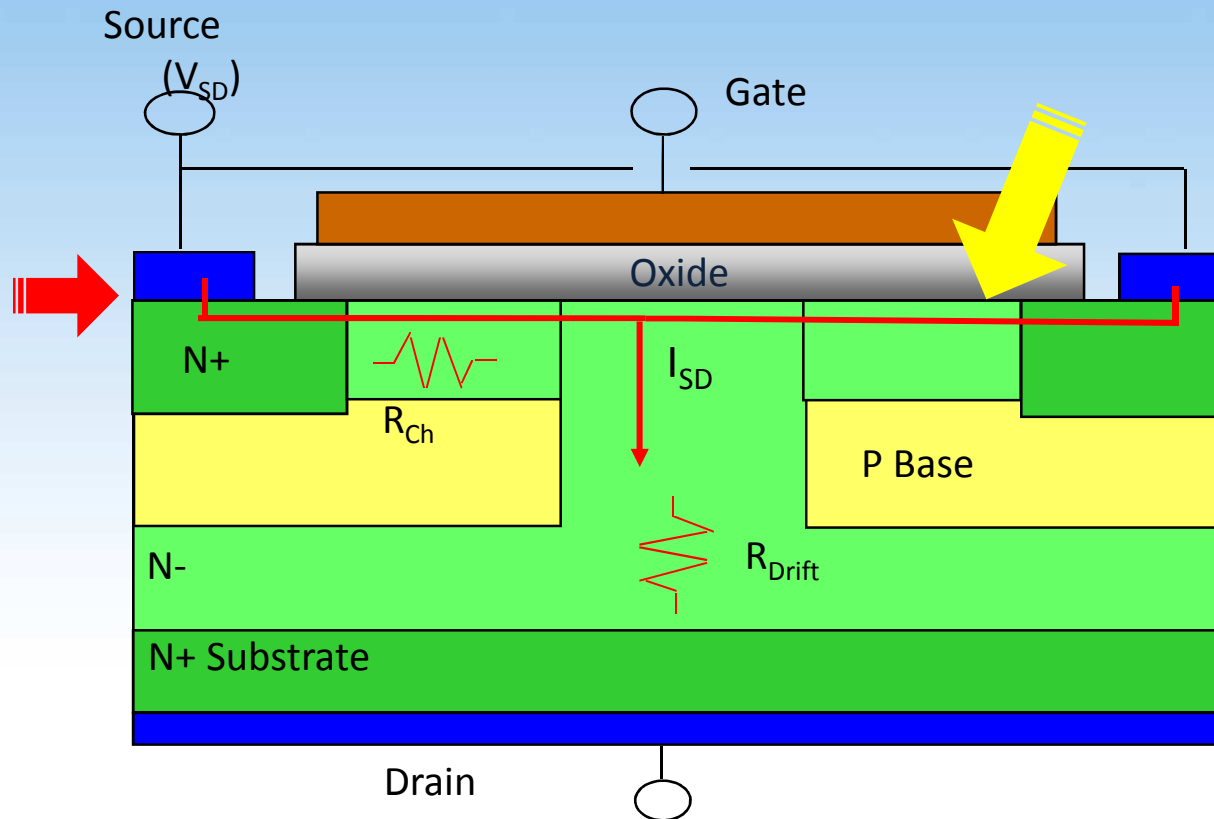
Small Device



*Big Device
Containing
176 Cells*



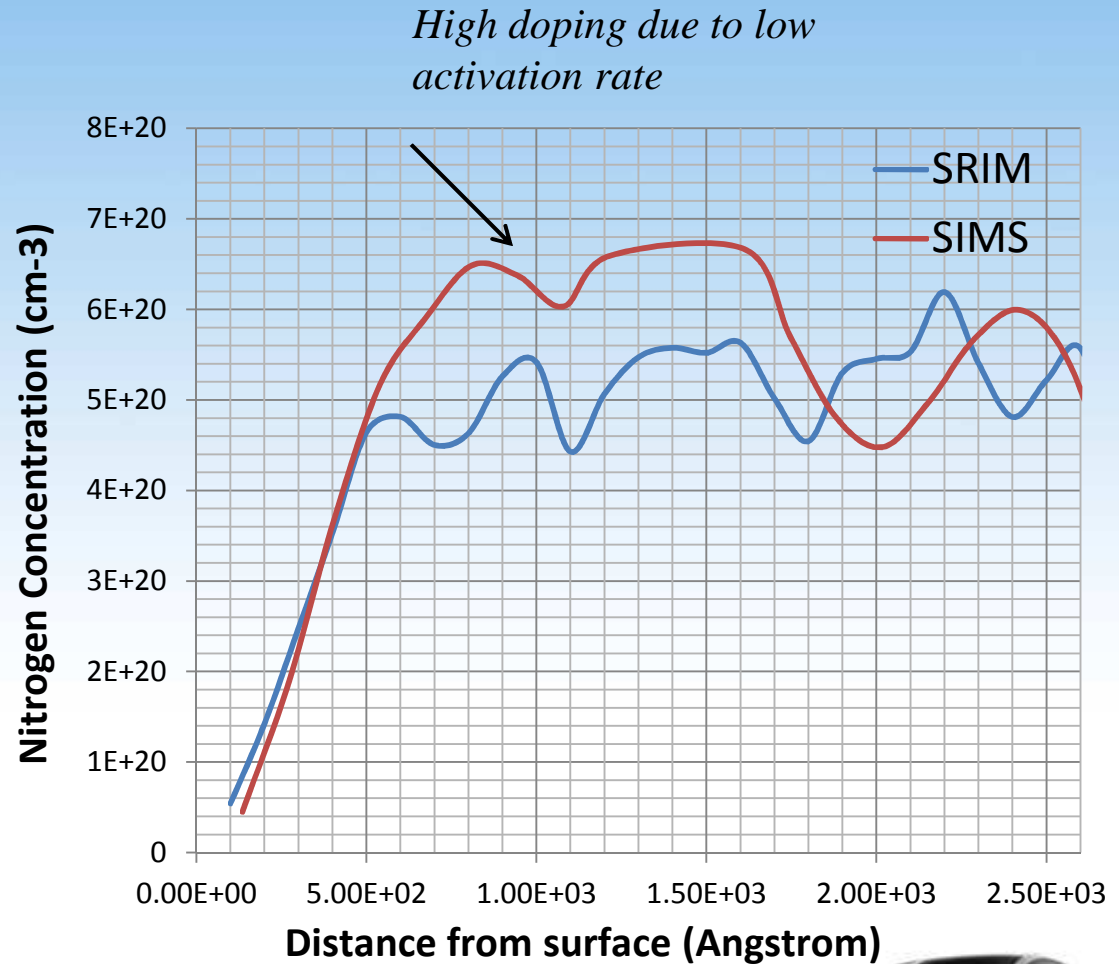
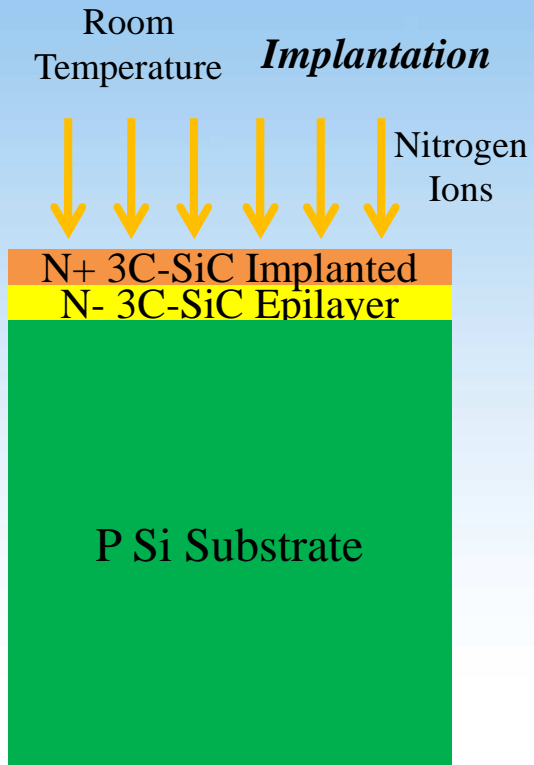
Lateral MOSFET



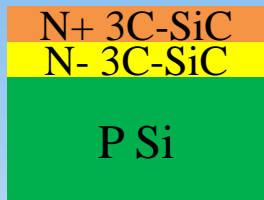
- Metal-semiconductor contacts
- SiC/SiO₂ interface



Ohmic Contact on N Type 3C-SiC

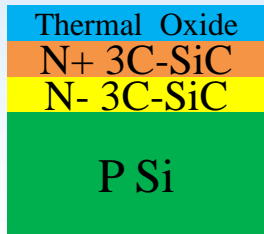


Ohmic Contact on N Type 3C-SiC



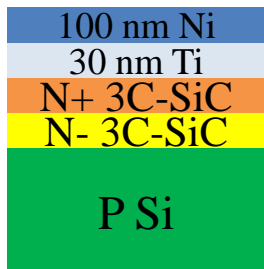
1 μm

Activated for 1 hour at 1300 °C in HighTech furnace

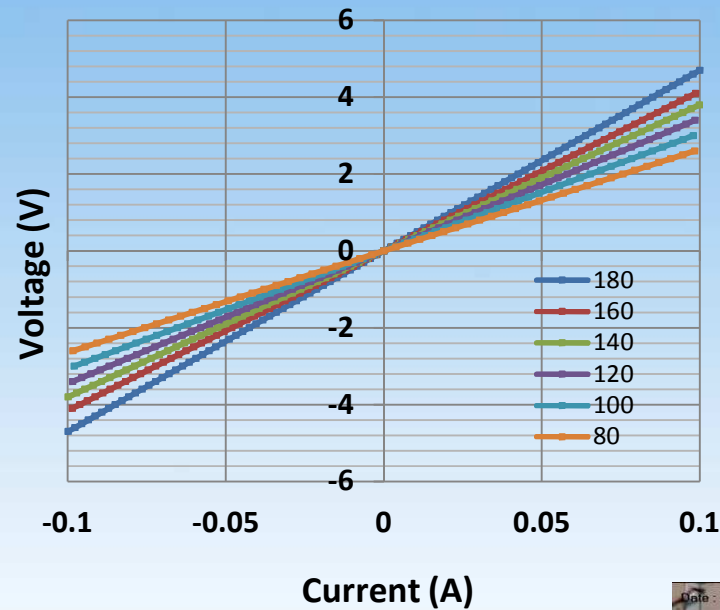


140 nm

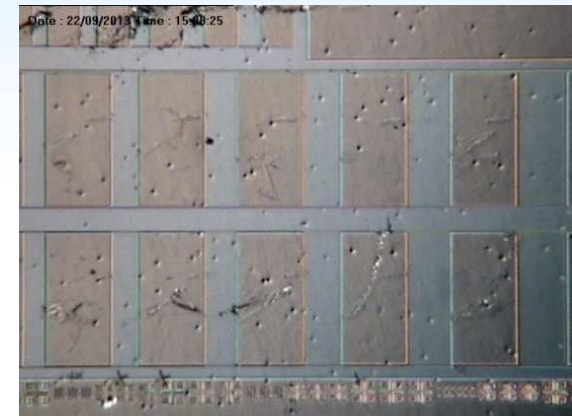
Oxidation lasted 2 hours at 1200 °C in HighTech furnace, oxygen flow 4 slm



Metallization happened at $2e-5$ Torr, annealed for 1 min at 1000 °C



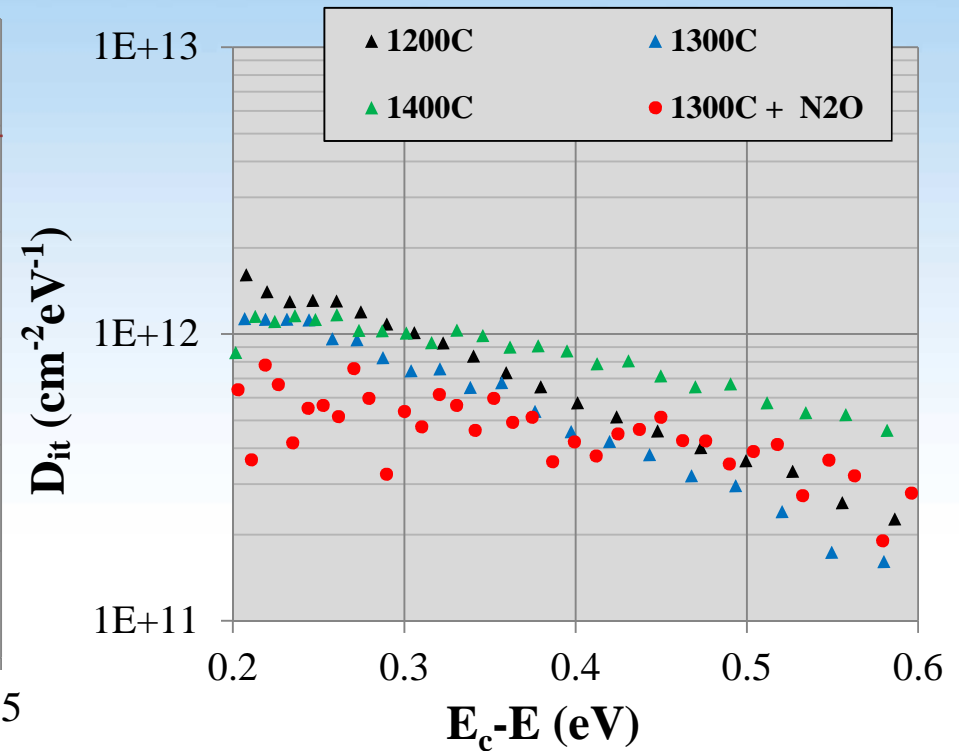
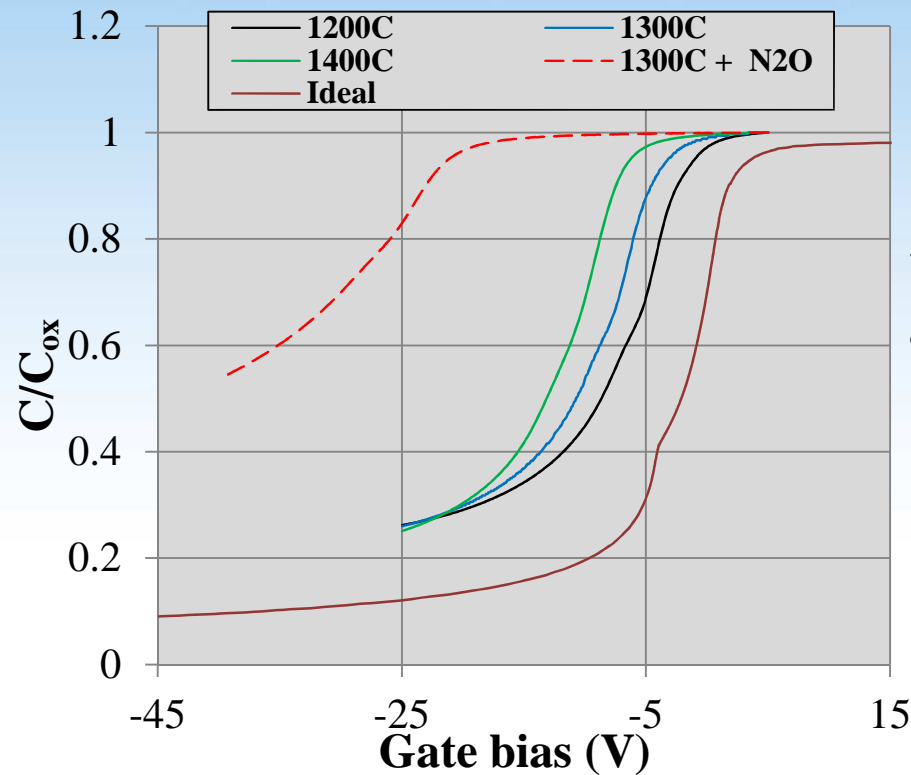
Resulting specific contact resistance $2e-5 \Omega.cm^2$.



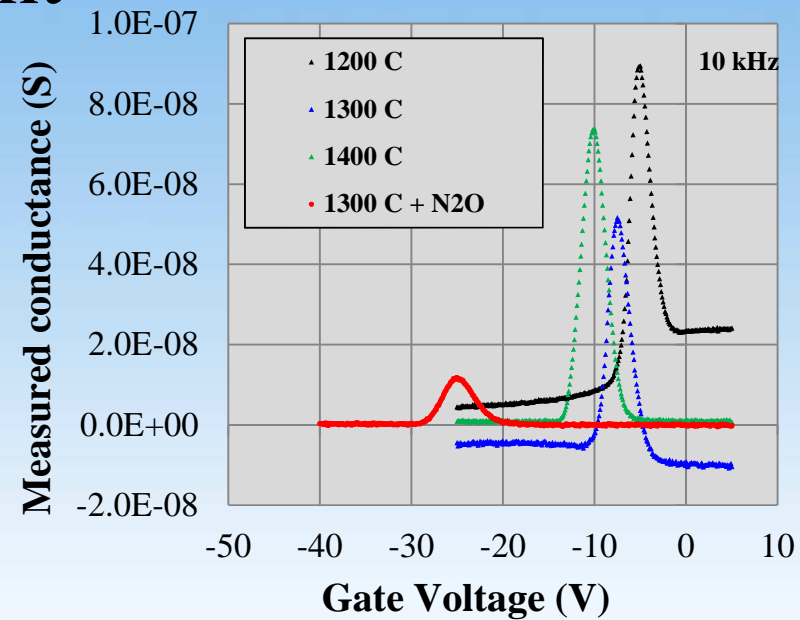
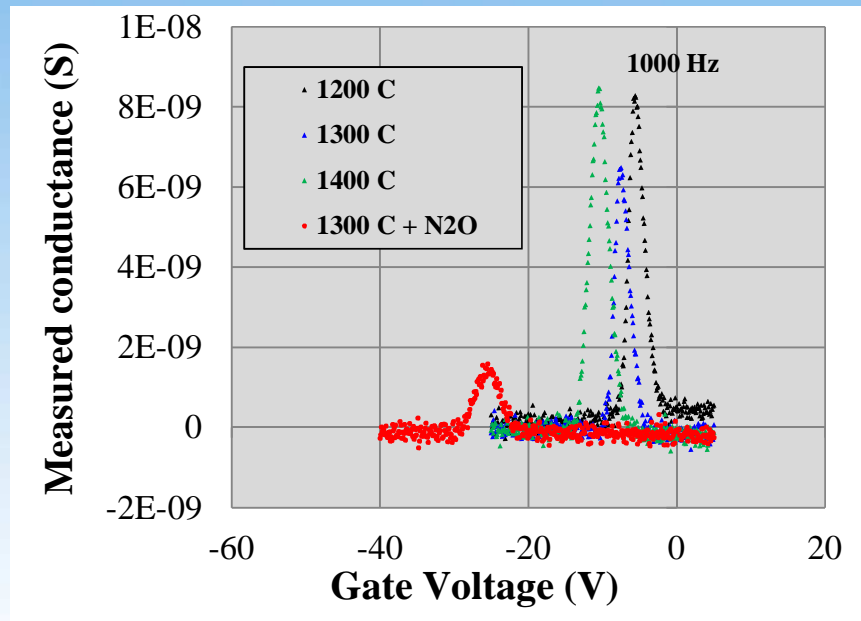
TLM feature under optical microscopy



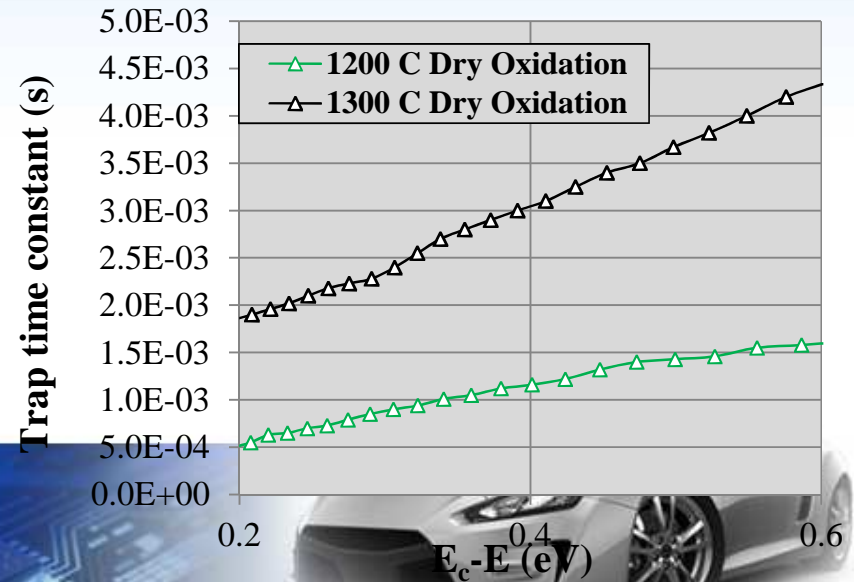
Effect of oxidation condition/passivation at the 3C-SiC/SiO₂ interface



Properties of interface traps- nature, time constant



Process	Flatband voltage (V)	Effective oxide charge
1200C oxidation	-4	1.07E+12
1300C oxidation	-6	1.60E+12
1400C oxidation	-8	2.69E+12
1300C (oxidation+N2O)	-22	4.02E+12



Future Plans

- Continue working on 3C-SiC Ohmic contact –more test structures
- Use modified MOS-C structure, look more into 3C-SiC oxidation post annealing and passivation methods
- Start the Lateral MOSFET design and simulation



Conferences/Papers



12th INTERNATIONAL SEMINAR ON POWER SEMICONDUCTORS
ISPS 2014, Prague



Thank You For Listening

