A LOW POWER, LOW PHASE NOISE FBAR OSCILLATOR

Authors: WEI-WEI CHENG [a]; SHU-RONG DONG [a]; YAN HAN [a]; HAI-FENG ZHOU [a]; SHI-HENG ZHAO [a]; HUI-JIN ZHANG [a]; XIAO-XIA HAN [a]
Affiliation: [a] Institute of Microelectronics and Optoelectronics, Zhejiang University, Hangzhou, P. R. China
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Abstract

A novel low power, low phase noise CMOS oscillator based on thin film bulk acoustic resonator (FBAR) is submitted in this paper, which aims at application in wireless sensor networks. This oscillator is designed as current-reuse configuration to reduce power dissipation. The simulation results show that the oscillator operating at 1.878 GHz consumes 1.8 mW with a low supply voltage of 900 mV. That is only a half of power consumption of the conventional topologies. Moreover, its phase noises are -107 dBc/Hz and -135 dBc/Hz at 10 kHz and 100 kHz offsets respectively, and its FOM is -238 dBc/Hz.
Keywords: FBAR; low power; low phase noise; oscillator

INTRODUCTION

Film Bulk Acoustic Resonator (FBAR), a thin film piezoelectric resonator based on bulk acoustic, is a good candidate of integrated mass sensor chip owing to its high operating frequency, very high Q factor (above 1000), integrated process and small size [1]. So FBAR mass sensor has increasingly been used in chemical, biological, liquid, gaseous environment [1, 2], which as, for example, a liquid sensor [3, 4, 5], a gas sensor [4, 5], a biosensor sensor [6, 7, 8, 9] or a DNA and protein detector [6], a mercury-ion detector [10], a sensor in viscous media [11], a glycerol detector [12], a explosive trace detector [13], or a localized-mass detector [14, 15]. As an important part of FBAR mass sensor, FBAR oscillator provides an amplified resonate frequency signal to sense mass change, thus it requires low phase noise. And while FBAR mass sensor is used in wireless sensor networks (WSN), it also needs radio frequency transceiver with an oscillator, such as FBAR oscillator with low power consumption [16, 17, 18, 19]. In the last few years, several efforts for FBAR oscillators with both CMOS integrated circuit and discrete circuit have been reported with impressive phase noise performance [2, 19, 20, 21, 22]. This paper presents a novel two-transistor oscillator topology that utilizes an on-chip FBAR as its series resonance circuit and a traditional LC tank as a parallel resonator.

THEORY, DESIGN AND SIMULATION

FBAR Model

The FBAR is composed of a thin piezoelectric film sandwiched by two metal electrodes. Considering its fabrication process being compatible with current standard CMOS technology, there are two main structures shown in Fig. 1, which are back-etching bulk silicon structure [19] and air gap structure [20]. In practice, the resonance characteristics of FBAR device are similar to quartz crystals with one series resonant frequency and one parallel resonant frequency. Its Q factor is mainly determined by the electrode material and the thickness, area, surface roughness, stress, and crystal orientation of the piezoelectric material [20, 23, 24, 25, 26].

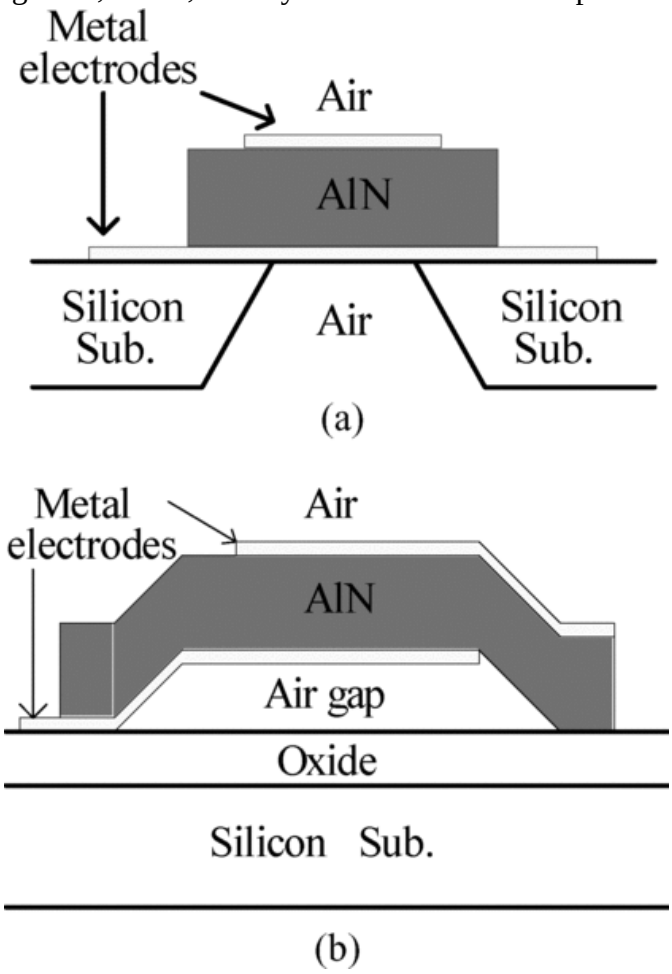

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Figure 1 (a) Cross-section of the FBAR, Bottom etching structure. (b) Cross-section of the FBAR, Air gap structure.

The MBVD (Modified Butterworth Van Dyke) equivalent circuit of FBAR is shown in Fig. 2, which includes a static capacitor C_0 and its loss R_0, mechanically dynamic capacitor C_m, dynamic inductor L_m, and dynamic loss R_m [27]. So FBAR has two resonant frequencies as the serial resonant frequency f_s and the parallel resonant frequency f_p. The L_m and C_m account for f_s, whereas L_m, C_m, and C_0 account for f_p. Then it is a narrow frequency band between f_s and f_p, in which the FBAR behaves like an inductor with high Q factor. Thus, this

characteristic leads to low power and high performance oscillators, coupled with good circuit design [28].

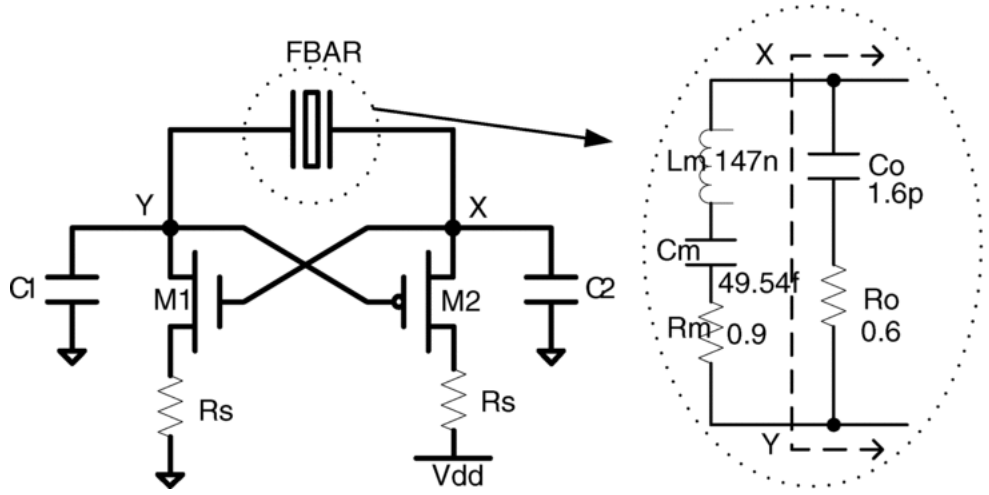

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Figure 2 Schematic of the FBAR oscillator and the equivalent circuit of FBAR.

Circuits Design

The FBAR oscillator circuit is designed as the current-reuse differential configuration structure, shown in Fig. 2. The usage of the current-reuse differential configuration structure is to reduce the current consumption, namely which obtains the same transconductance for oscillator but at a decreased power dissipation compared to standard topologies [29]. As in this FBAR oscillator circuit,the negative conductance is provided by the cross-connected pairs of transistors M1 and M2, which compensates the losses in the FBAR. Ordinarily, the cross-connected transistors of the traditional differential oscillator consist of a pair of NMOSs or a pair of PMOSs in order to generate the negative conductance, while the cross-connected transistors of the proposed FBAR oscillator is composed of a NMOS and a PMOS; and the transistors of the former switch alternately, while the transistors of the latter switch simultaneously. Therefore, comparing with the conventional structures, the proposed configuration can reduce the power consumption by half and provide the same negative conductance. Furthermore, the output voltage is biased at $V_{dd}/2$ to maximize the allowable voltage swing.

With $R_s = 0$, the schematics and corresponding large-signal equivalent circuits during each half period of operation (when the voltage at node X is high and low) are shown in Fig. 3 to explain the operation of the proposed FBAR oscillator, where C_1 and C_2 represent the parasitical capacitances of electrodes, MOS transistors, pads and interconnects. As shown in the figure, during the first half-period (when the voltage at node X is high), the transistors M1 and M2 are on and the current flows from V_{dd} to ground through the FBAR.; and during the second half-period (when the voltage at node X is high), the transistors are off and the current flows in the opposite direction through the capacitors C_1 and C_2. In fact, in the former half-period of oscillation, the PMOS and the NMOS operate in triode mode near the peak of the voltage swing. In this case, the output voltage swing is limited by the supply voltage, this region of operation is consequently known as the voltage-limited regime; on the other hand, in the latter half-period of oscillation, the voltage swing across the FBAR is not limited and

can lead to a voltage swing which is higher than the supply voltage.

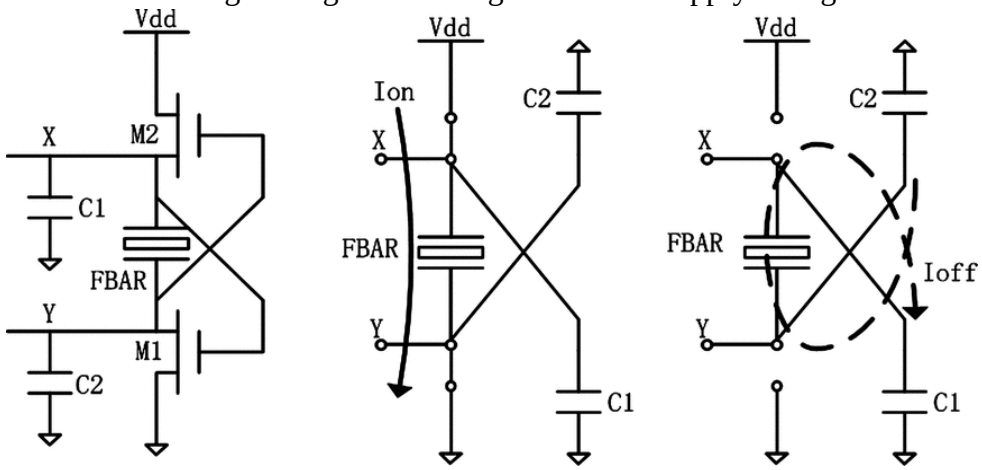

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Figure 3 The FBAR oscillator operates with $R_s = 0$ during each half period.

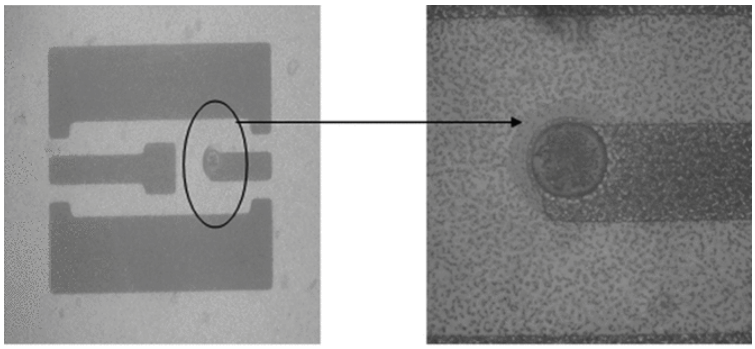
Capacitors C_1 and C_2 transform g_m which is the transconductance of the amplifier into a negative resistance $-g_m/\omega^2 C_1 C_2$ at the frequency ω. Accordingly higher current consumption is required to obtain higher negative resistance, considering that g_m is proportional to the device current. The impedance looking across node X and node Y is given as [28]

$$Z_{XY} = \frac{Z_1 Z_2 + Z_2 Z_3 + g_m Z_1 Z_2 Z_3}{Z_1 + Z_2 + Z_3 + g_m Z_1 Z_2}$$ where $Z_1 = 1/j\omega C_1$, $Z_2 = 1 j\omega C_2$, $Z_3 = R_0 + 1/j\omega C_0$. To ensure the oscillator startup, the real part of the impedance Re $[Z_{XY}]$ is typically about two times higher than $-R_m$. When the output voltage swing increases to the sufficiently large amplitude, M1 and M2 are pushed into gain compression, moreover, g_m and Re $[Z_{XY}]$ are reduced. Steady state oscillation is not achieved until the large signal Re $[Z_{XY}]$ is equal to $-R_m$.

Fabrication and Simulation

FBAR based on air bag reflector is fabricated on the silicon wafer, shown in Fig. 4(a). FBAR resonator curve is measured and shown in Fig. 4(b). Its resonating frequency is not very located at the designed range. Owing to no equipment to adjust resonating frequency and according process, we can not finish FBAR oscillator as design. We extracted FBAR

parameters in the model MBVD and simulated this FBAR oscillator based on MBVD model.



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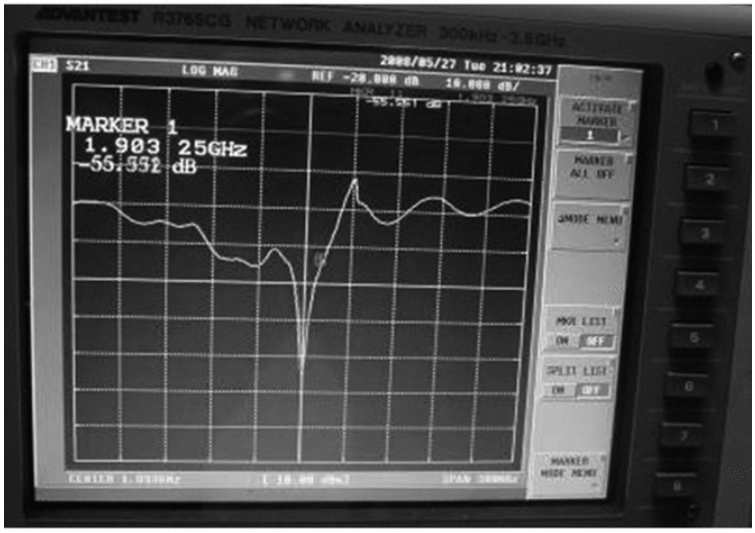

(b)

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Figure 4 (a) Chip-photo of FBAR. (b) Measured resonator frequency of FBAR.

The harmonic characteristics are effectively improved by developing the current-reuse differential configuration. Figure 5(a) shows the voltage swing at node X of the circuit with $R_s = 0$ in Fig. 2, and it illustrates that the output voltage swing of X node is beyond the supply voltage, thereby the drain-source voltage of M1 drops significantly, which results in the voltage-waveform distortion, namely the large drop in dynamic current during the first half-period leads to voltage-waveform distortion. Meanwhile, the oscillator circuit enters the voltage-limited mode, which causes that the NCR (noise-to-carrier ratio) increases with the increase of the inductance, and the inductance is wasted while NCR becomes higher, furthermore it is a disadvantage to noise suppression [30]. Figure 5(b) shows the result of PSS (periodic-steady-state) analysis, which represents the output harmonics. The 2nd order harmonic is -30.5dB which is a high value, so it is not suitable to generate a balanced differential voltage swing. In practice, the problem of distortion is solved by adding a series resistor R_s which controls the DC current as well as the peak dynamic current of the FBAR oscillator. By regulating the value of the resistor R_s to degrade the changes of the dynamic

current, the circuit can operate in a current-limited mode consequently.

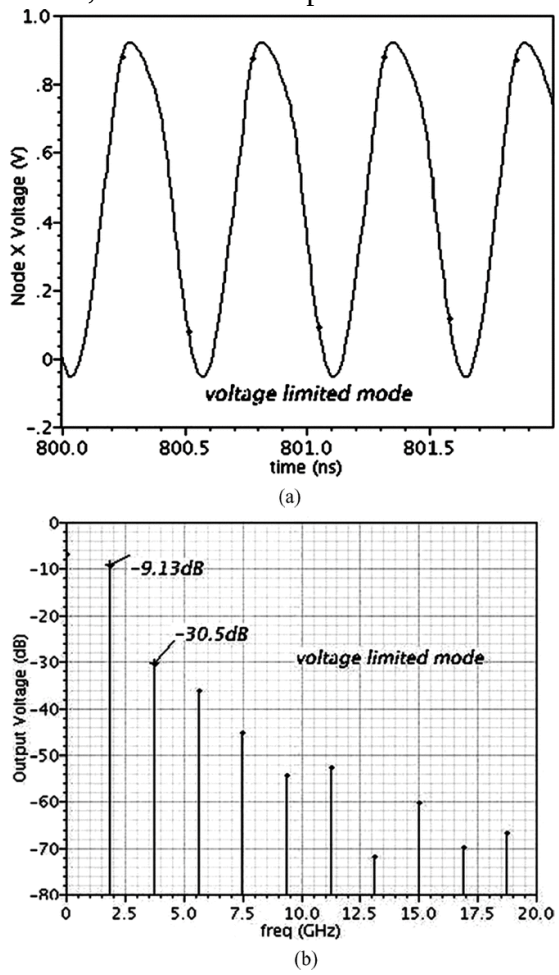

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Figure 5 (a) Voltage limited mode (Rs = 0), Output voltage waveform. (b) Voltage limited mode (Rs = 0), The PSS response.

In view of the balance of FBAR oscillator, the resistors are connected to both drains of M1 and M2. Then the circuit is in the current-limited mode, and the output voltage swing is symmetric and represents well-balanced behavior during whole period, which is shown in Fig. 6(a), where the voltage swing is 70-850 mV, which contributes to the reduction of the harmonic noise of the whole circuit [30]. Figure 6(b) also shows the results of PSS analysis

of the modified oscillator circuit, and the 2nd order harmonic is reduced to -39.5 dB.

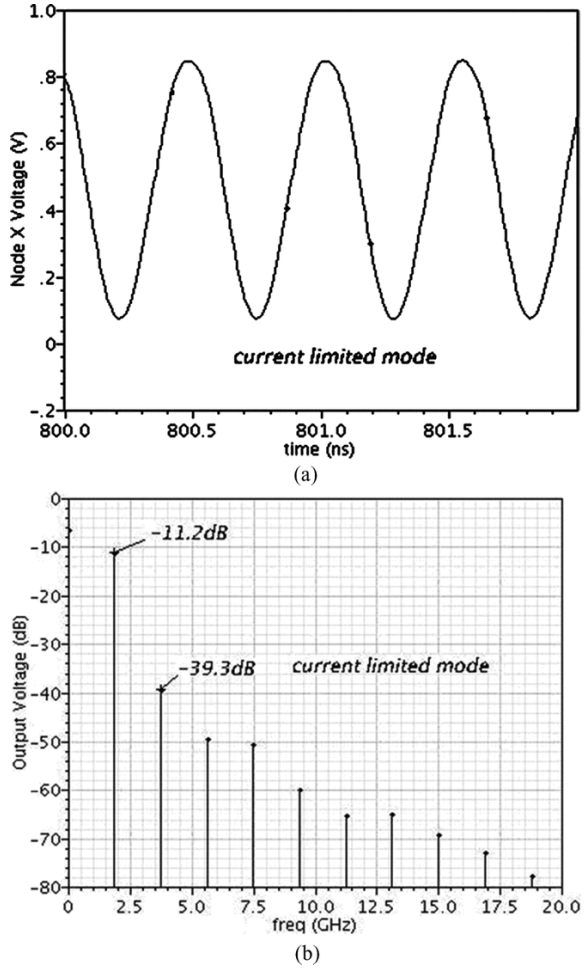

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Figure 6 (a) Current limited mode (Rs≠0), Output voltage waveform. (b) Current limited mode (Rs≠0), The PSS response.

Unlike the conventional oscillator, the FBAR-based oscillator with current-reuse differential configuration operates in the mode that the transistors switch alternately, and switch on and off at the same time, which not only reduces the power consumption but also improves the noise performance [29]. Figure 7 shows the simulated values of phase noise for the FBAR oscillator operating at 1.878 GHz, which are -107 dBc/Hz and -135 dBc/Hz at 10 kHz and 100 kHz frequency offset respectively. This low phase noise attributes to the high Q-factor of FBAR and the work mode that the circuit works only in half period so that the noise power generated by the MOS transistors as the main noise source is reduced by a half comparing

with other oscillators.

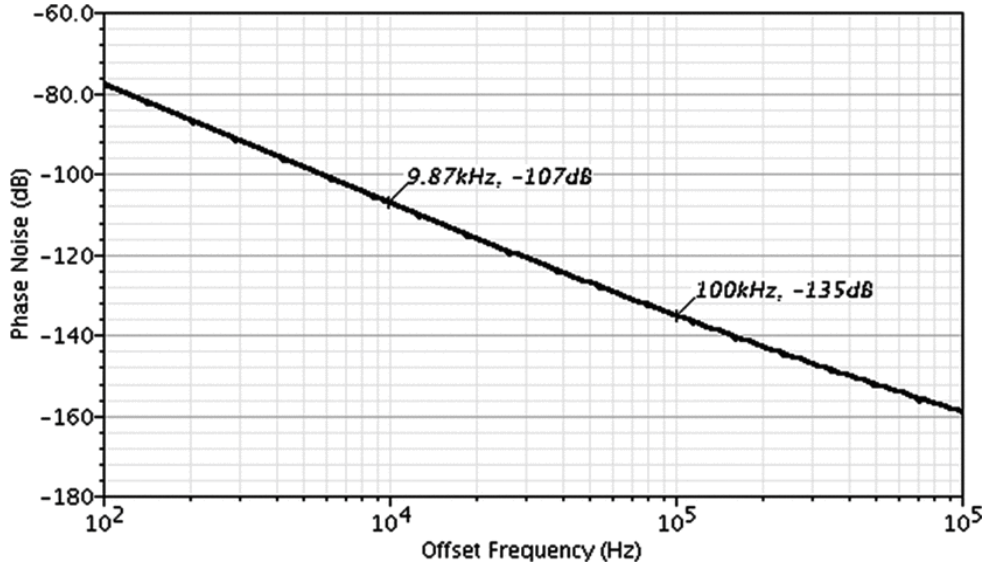

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Figure 7 Phase noise of the FBAR oscillator.

Usually, the figure-of-merit (FOM) which is the benchmark of the performance of oscillator is defined as [2]

$$\mathrm{FOM} = L\{f_{\mathrm{offset}}\} - 10\log\left(\frac{f_{\mathrm{osc}}}{f_{\mathrm{offset}}}\right)^2 + 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right)$$

where P_{DC} is the power consumption of oscillator, and $L\{f_{offset}\}$ is the phase noise of the oscillator at an offset frequency f_{offset} from its resonant frequency f_{osc}, Oscillating at 1.878 GHz, the FBAR oscillator is self-biased by 900 mV supply and dissipates 1.8 mW, thus the FOM of the FBAR oscillator is -238 dBc/Hz, and this value is much better than the ones of the on-chip LC oscillator and other FBAR oscillators with different structures: [18] presented the phase noise performance of -103 dBc/Hz and 100 kHz in 2005; [19] presented the phase noise performance of -98 dBc/Hz and -120 dBc/Hz at 10 kHz and 100 kHz in 2005; [20] presented the phase noise performance of -144.1 dBc/Hz and -149.6 dBc/Hz at 1 MHz and 3 MHz in 2006; [21] presented the phase noise performance of -110 dBc/Hz at 1 MHz in 2007; [22] presented the phase noise performance of -97 dBc/Hz at 10 kHz in 2008; [2] presented the phase noise performance of -125 dBc/Hz at 100 kHz in 2008.

This low power, low phase noise oscillator can be employed widely. The digital data can be modulated onto the RF carrier directly by cycling "on" and "off" states of the FBAR oscillator to apply FBAR oscillator to both the mass sensor and the radio frequency front-end of wireless sensor networks. Incidentally, with a variable-capacitance diode attached, its application is widen as a voltage-controlled oscillator with high performance. By combining the high Q factor FBAR with advanced CMOS process, low-power highly-integrated and high performance can be implemented.

CONCLUSION

A CMOS oscillator based on FBAR operating at 1.878 GHz is designed as the current-reuse configuration presented in this paper. This FBAR oscillator has ultra-low power consumption and low phase noise, simulation results show that its power consumption is 1.8 mW and its phase noise is -107 dBc/Hz@10 kHz and -135 dBc/Hz@100 kHz respectively with the voltage supply of 900 mV. Moreover, its FOM is -238 dBc/Hz, which is good FOM in the state-of-the-art oscillators.

ACKNOWLEDGMENTS

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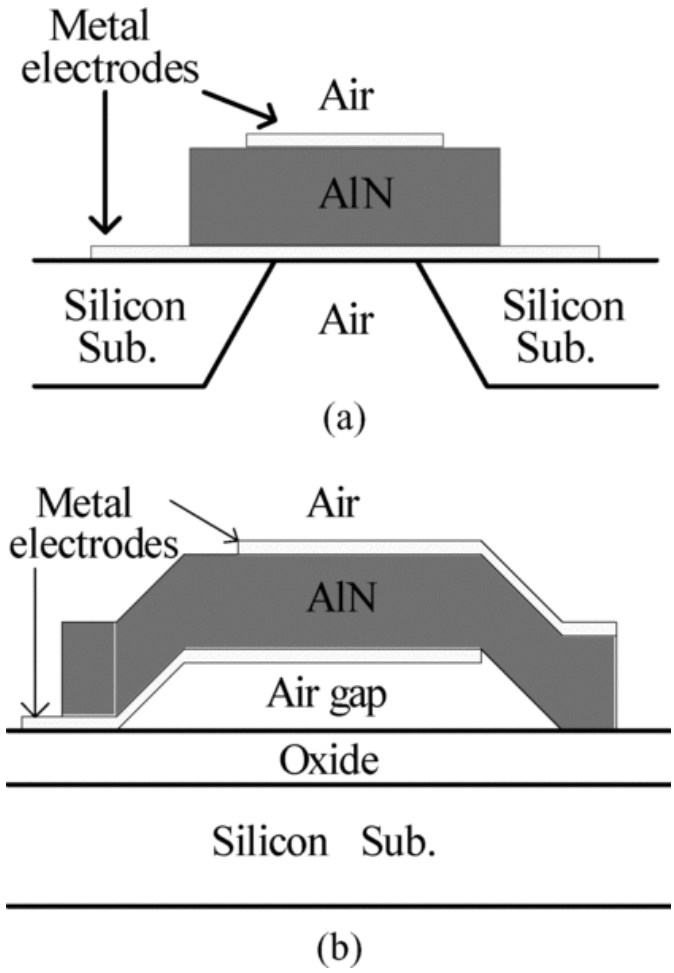

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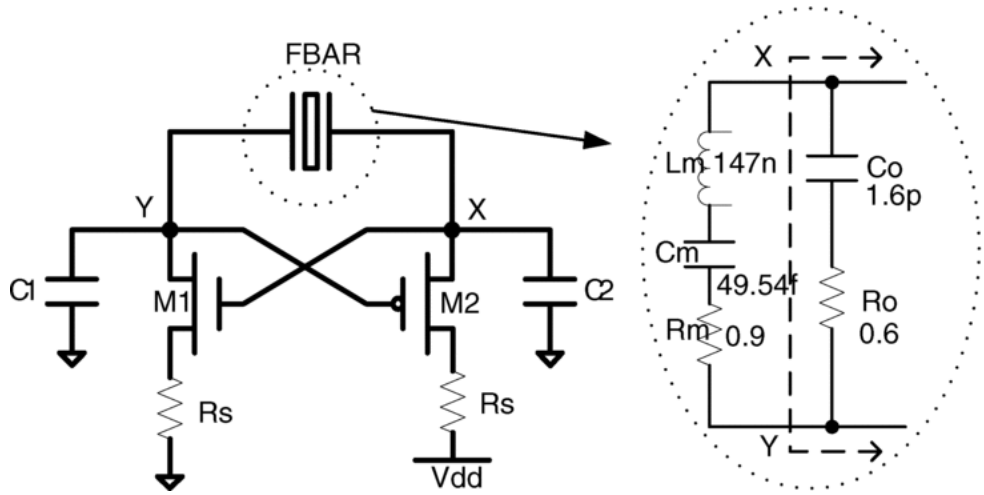

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Figure 2 Schematic of the FBAR oscillator and the equivalent circuit of FBAR.

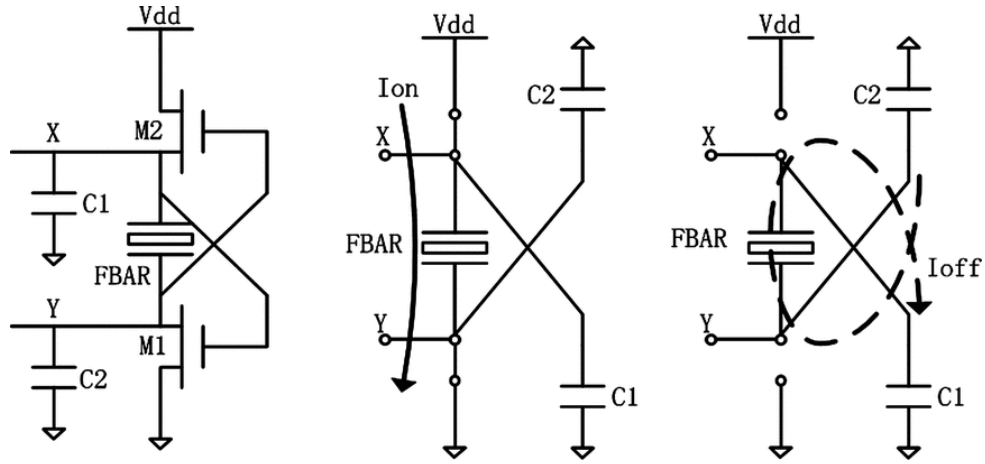

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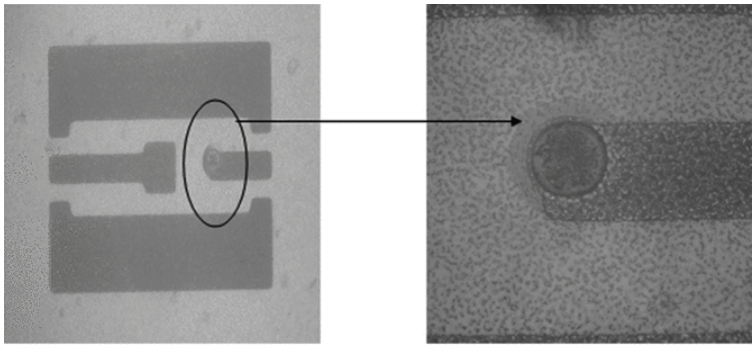
Figure 3 The FBAR oscillator operates with $R_s = 0$ during each half period.



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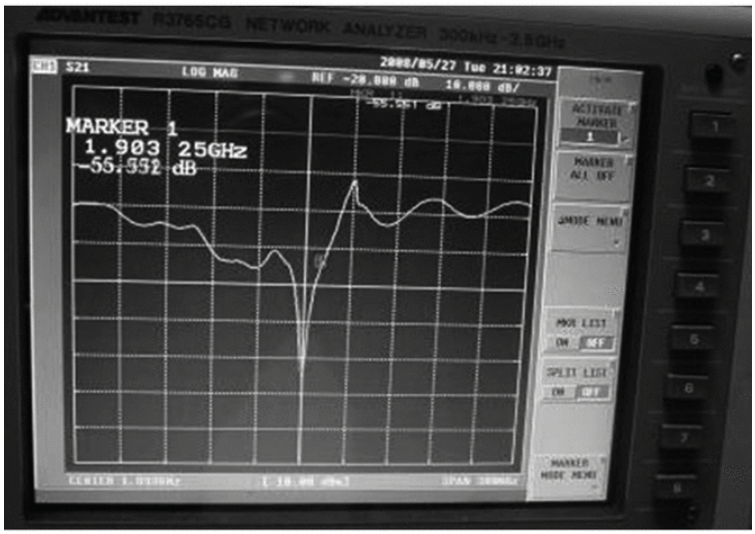

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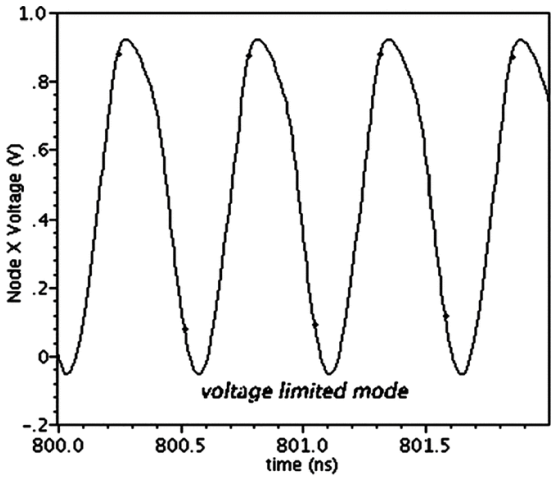
Figure 4 (a) Chip-photo of FBAR. (b) Measured resonator frequency of FBAR.



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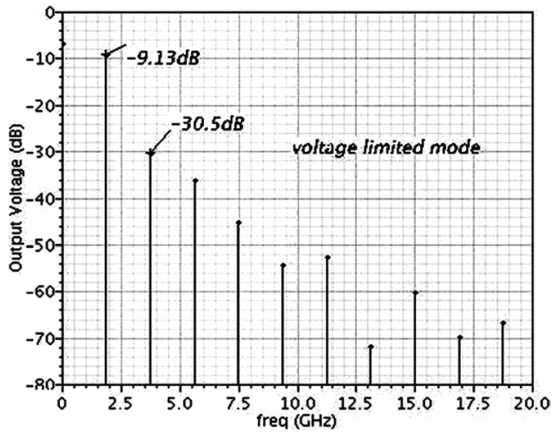

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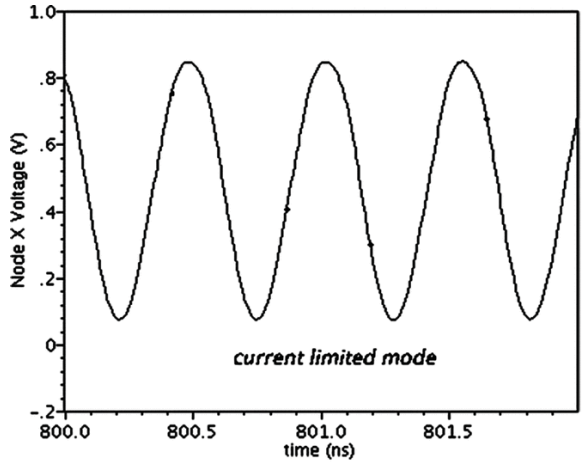
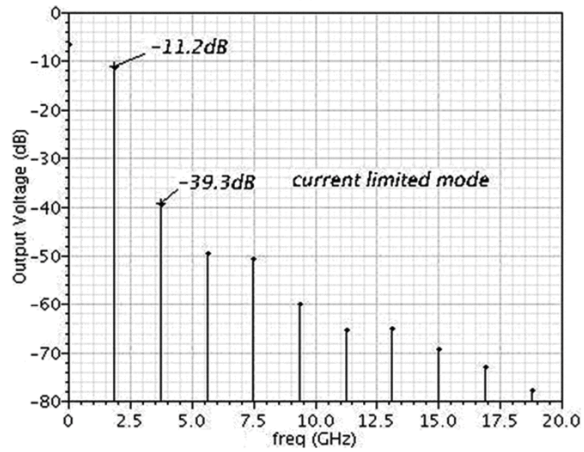
Figure 5 (a) Voltage limited mode (Rs = 0), Output voltage waveform. (b) Voltage limited mode (Rs = 0), The PSS response.



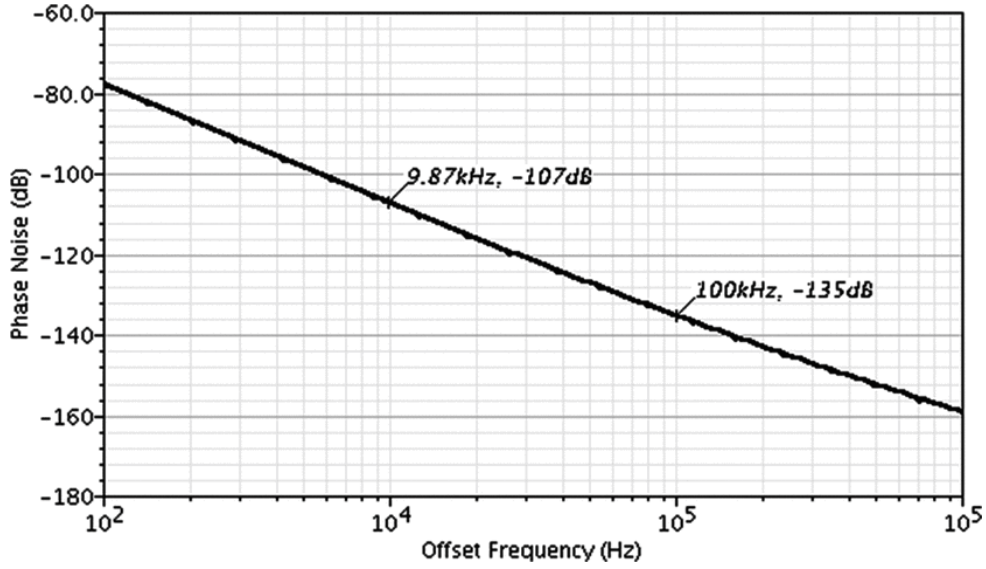
(a)



(b)

[Enlarge Image]

Figure 6 (a) Current limited mode (Rs≠0), Output voltage waveform. (b) Current limited mode (Rs≠0), The PSS response.



[Enlarge Image]

Figure 7 Phase noise of the FBAR oscillator.