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REVIEW

Materials Science Challenges to Graphene Nanoribbon Electronics

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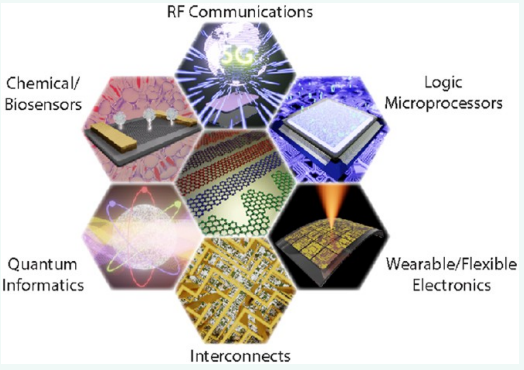
ABSTRACT: Graphene nanoribbons (GNRs) have recently emerged as promising candidates for channel materials in future nanoelectronic devices due to their exceptional electronic, thermal, and mechanical properties and chemical inertness. However, the adoption of GNRs in commercial technologies is currently hampered by materials science and integration challenges pertaining to synthesis and devices. In this Review, we present an overview of the current status of challenges, recent breakthroughs toward overcoming these challenges, and possible future directions for the field of GNR electronics. We motivate the need for exploration of scalable synthetic techniques that yield atomically precise, placed, registered, and oriented GNRs on CMOS-compatible substrates and stimulate ideas for contact and dielectric engineering to realize experimental performance close to theoretically predicted metrics. We also briefly discuss unconventional device architectures that could be experimentally investigated to harness the maximum potential of GNRs in future spintronic and quantum information technologies.



KEYWORDS: *one-dimensional carbon, semiconductors, low-power logic, radio frequency devices, CMOS technologies, more than Moore, monolithic 3D integration, tunnel field-effect-transistors, contact engineering, high-κ dielectrics*

INTRODUCTION

For over 50 years, unparalleled strides in microelectronics have been fueled by relentless miniaturization[1] and innovation in interconnect, dielectric, and contact materials.[2,3] Meanwhile, the composition of the semiconductor channel of field-effect transistors (*e.g.*, Si and III−V compounds in logic and high-speed communication devices, respectively) has remained relatively unchanged. Now, more than ever, there is an urgent need for disruptive materials that can complement or even replace these conventional semiconductors in field-effect transistor (FET) devices in order to increase performance—as gains derived from dimensional scaling diminish because of short-channel effects[4] and the limits of lithography.[5]

The International Roadmap for Devices and Systems (IRDS)[6] has identified several promising alternatives to Si such as III−V compound semiconductors (*e.g.*, InAs, InGaAs, *etc.*),[7] Ge,[8] SiGe,[9] carbon nanotubes (CNTs),[10] graphene nanoribbons (GNRs),[11] and layered transition metal dichalcogenides (TMDCs) (*e.g.*, MoS_2 and WSe_2). GNRs, which are narrow strips of graphene, are especially appealing for logic microprocessors because their electronic properties have the potential to exceed those of Si (*e.g.*, high carrier mobility, current-carrying capacity, and saturation velocity), thereby enabling higher performance at a lower power supply.[12] In addition to logic, semiconducting GNRs are also attractive for low-power radio frequency (RF) technologies, and for a range of emerging devices for thin-film electronics (*e.g.*, flexible devices and sensors), spintronics, and quantum informatics.[13−22]

However, the adoption of GNRs in transistor technologies is inhibited by a range of fundamental synthesis, integration, and materials science challenges. This paper reviews the electronic properties of GNRs, the production of GNRs, and the materials science challenges that must be overcome before GNRs can be exploited in commercial technologies. While GNRs are also being investigated for interconnects,[23−27] photovoltaics, and optoelectronics,[28−30] in this Review, we primarily focus on the application of GNRs as a channel material in transistors.

GNRs can be primarily classified based on their width and the crystallographic direction along which they are sliced from

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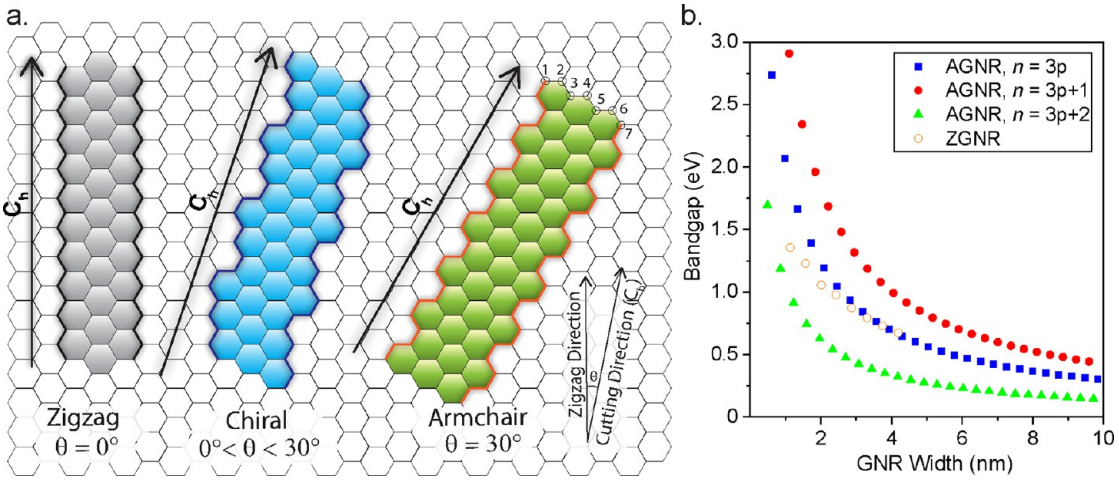

Figure 1. (a) Classification of GNRs based on the angle between the GNR long axis, defined by the vector C_h, and the zigzag crystallographic direction of the graphene lattice. (b) Theoretically predicted band gaps of armchair GNRs (AGNRs) and zigzag GNRs (ZGNRs) in a vacuum as a function of width. Data extrapolated from ref 35.

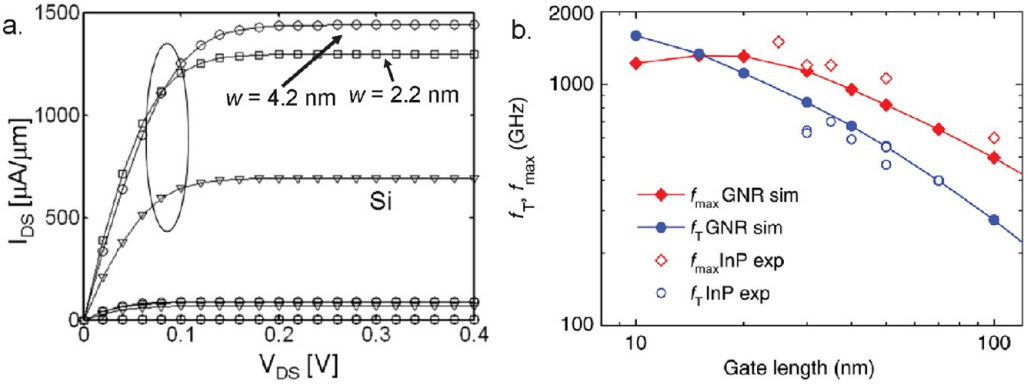

Figure 2. Theoretically projected performance of GNR FETs for logic and RF applications. (a) Plot of drain saturation current density versus drain voltage for 2.2 and 4.2 nm wide ideal ballistic GNR MOSFETs compared to the ballistic Si MOSFET. Reproduced with permission from ref 57. Copyright 2007 IEEE. (b) Simulated cutoff and maximum oscillation frequencies versus gate length for an n = 16 armchair GNR MOSFET compared to the experimental performance of InP high-electron-mobility transistors. Reproduced with permission from ref 62. Copyright 2017 Wiley-VCH.

a graphene sheet, *viz.*, zigzag (*i.e.*, ribbon long edge perpendicular to C−C bonds), armchair (*i.e.*, ribbon long edge parallel to C−C bonds), or chiral (Figure 1a). Both width and direction profoundly impact the GNR band structure, leading to varied electronic properties.[31−33] Unlike graphene, but similar to CNTs, GNRs can exhibit tunable, technologically relevant band gaps $\gg k_BT$ at room temperature, where k_B is the Boltzmann constant, and T is temperature.[34−37] Zigzag and armchair GNRs have been experimentally explored most often because these edges tend to be favored in synthesis, and the largest band gaps occur for armchair GNRs. The electronic properties of GNRs are further classified by width, w. For example, based on the number of rows of carbon atoms (n) along their width, armchair GNRs are classified into $n = 3p$, $3p + 1$, and $3p + 2$ families, where p is an integer. Theoretical calculations[35,38] and experimental data[39,40] indicate that the band gap (E_g) of armchair GNRs decays inversely with width ($E_g \propto w^{-\alpha}$, $\alpha \approx 1$), but with magnitude, that depends on the width family, with the $3p + 1$ family exhibiting the largest band gaps. Although band gaps can be significantly perturbed by the surrounding media due to renormalization of quasiparticle energy levels, roughly speaking, for armchair GNRs isolated in vacuum, $0.8 \le E_{g,3p+1} \le 3$ eV, $0.5 \le E_{g,3p} \le 2$ eV whereas $0.25 \le E_{g,3p+2} \le 1$ eV (Figure 1b) for widths ranging from 1.0 to 5.0 nm.[35,41] Narrow zigzag GNRs ($w < 5$ nm) are also predicted to exhibit an inverse band gap relationship with width wherein $0.4 \le E_g \le 1.3$ eV,[35] whereas wider zigzag GNRs are expected to exhibit a small, width-independent band gap.[33,42,43] Additionally, zigzag GNRs exhibit peculiar localized edge states, which are absent in armchair GNRs.[44] These localized states at the edges of zigzag GNRs couple ferromagnetically at the edges and may couple antiferromagnetically or ferromagnetically between opposite edges (depending on carrier density),[43,45−47] and coherent topological modification, *e.g.*, *via* introduction of defects and passivation with functional groups is expected to impart stable edge magnetism and half-metallicity in such GNRs.[48−55]

Thus, depending on the desired E_g, GNRs can be adapted into a myriad of applications ranging from high-performance logic to optoelectronics. For instance, $3p + 1$ armchair GNRs with $w < 2$ nm are potential candidates for short-channel FETs (channel length, $L_{ch} < 20$ nm) wherein a large E_g (nominally > 0.8 eV)[56] would be needed to suppress source-to-drain tunneling. Conversely, wider $3p$ or $3p + 1$ armchair GNRs with $2 \le w \le 5$ nm ($0.2 \le E_g \le 1$ eV) and sub-5 nm wide zigzag GNRs are suited for low-power analog/RF applications

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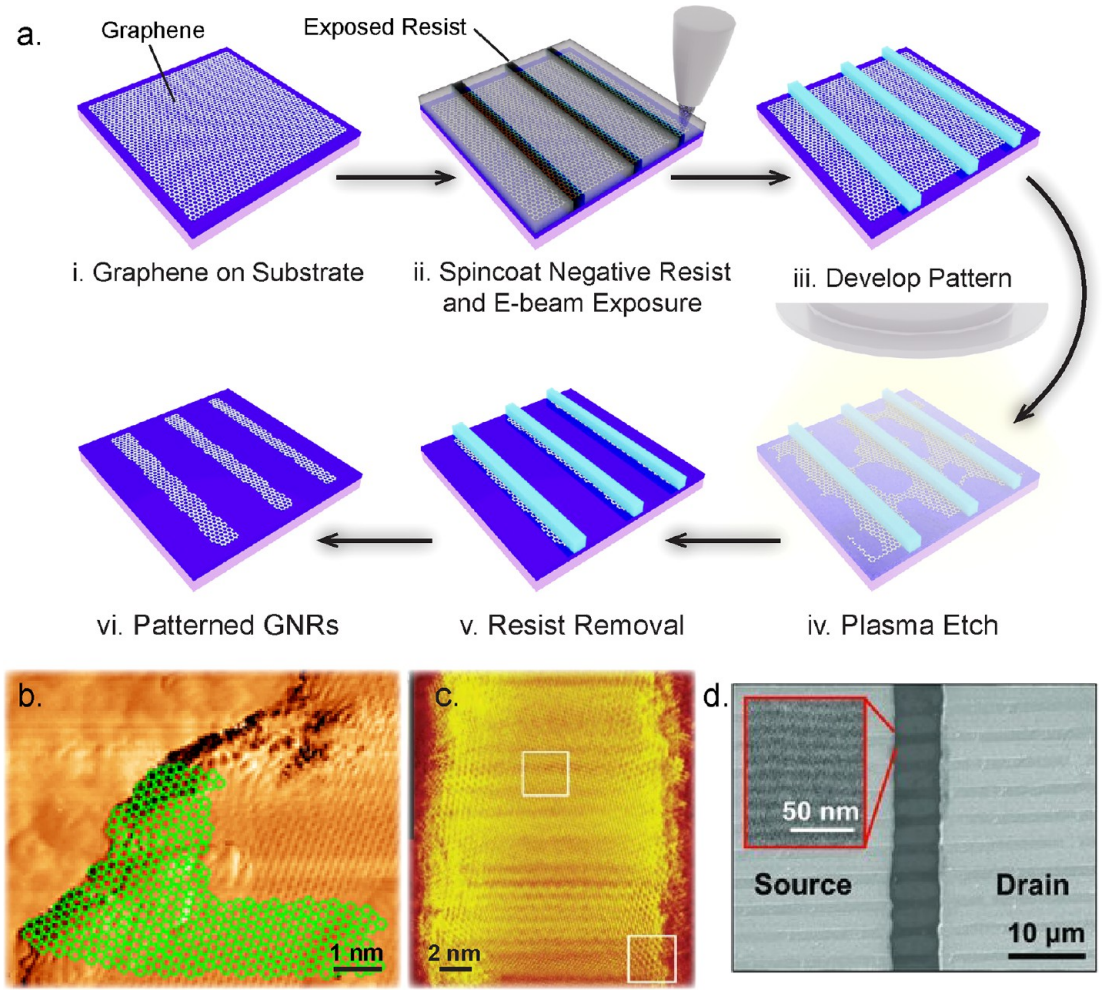

Figure 3. Top-down methods for GNR fabrication. (a) Overview of sequence of steps to produce GNRs by electron-beam lithography. (b) STM of GNR edges on SiC fabricated by electron-beam lithography and reactive-ion etching of monolayer graphene. Reproduced with permission from ref 111. Copyright 2016 Institute of Physics. (c) Atomic-resolution STM topography image of GNRs fabricated by STM lithography. Reproduced with permission from ref 105. Copyright 2008 Springer Nature. (d) Sub-10 nm wide GNR arrays fabricated using block copolymer lithography. Reproduced with permission from ref 97. Copyright 2013 Wiley-VCH.

wherein the lower E_g is expected to maximize on-state conductance and therefore speed of operation.[41,57] Even wider armchair and zigzag GNRs with $5 \leq w \leq 10$ nm are likely to be suited for additional applications requiring high conductance, such as interconnects, optoelectronics, printed electronics, quantum, and high-power devices.[28,57−60]

At the forefront of potential applications of GNRs are logic technologies, which are currently dominated by Si-based FinFET and silicon-on-insulator (SOI) technologies.[61] Here, semiconducting armchair GNRs with sub-5 nm widths are promising candidates due to their potential to achieve twice as high on-current density and up to 10−15% lower subthreshold swing than Si in metal−oxide−semiconductor (MOS) FETs at 10 nm gate length (Figure 2a).[57,62] For a comparable channel thickness ($t_{ch} \sim 1$ nm), GNRs exhibit nearly 100 times higher carrier mobility than ultrathin channels of bulk semiconductors such as Si or Ge. The atomically thin body of GNRs also enables superior electrostatic gate modulation, thereby reducing short-channel effects, improving the energy-delay product, and making GNRs promising candidates in ultra-scaled FETs.[63−65] Furthermore, band gap engineering of GNRs affords an additional degree of freedom to circuit designers to tailor GNR FETs for both high-performance and low-power applications.[66] As a consequence of graphene's semimetallic, gapless band structure, graphene FETs exhibit low conductance modulation—precluding their use in logic—and exhibit poor current saturation and large output conductance, resulting in degraded RF performance (*i.e.*, poor oscillation frequencies and gains). GNR FETs, however, are expected to exhibit cutoff frequencies (f_T) and oscillation frequencies (f_{max}) approaching the terahertz (THz) range, nearly 2−3 times higher than state-of-the-art Si RF MOSFETs and comparable to III−V high-electron-mobility transistors (*e.g.*, GaAs, InP, GaN, *etc.*; Figure 2b).[62,67,68] Moreover, unlike III−V semiconductors, GNRs are compatible with complementary MOS (CMOS)[69] and can be directly integrated on group IV semiconductors such as Ge, SiC, and Ge-on-Si[70−74] without the constraints of needing a lattice-match, which can improve functionality and performance and reduce costs of integrated RF/analog and logic system-on-chip (SoC) technologies. Considering the lower barrier to entry for new materials in analog/RF electronics compared to logic, GNRs might enable breakthrough technologies demanding high speed and linearity, *e.g.*, 5G, 60 GHz Wi-Fi, and wireless video that operate in millimeter-wave frequencies.[14,75] Additionally, the excellent mechanical strength and flexibility of

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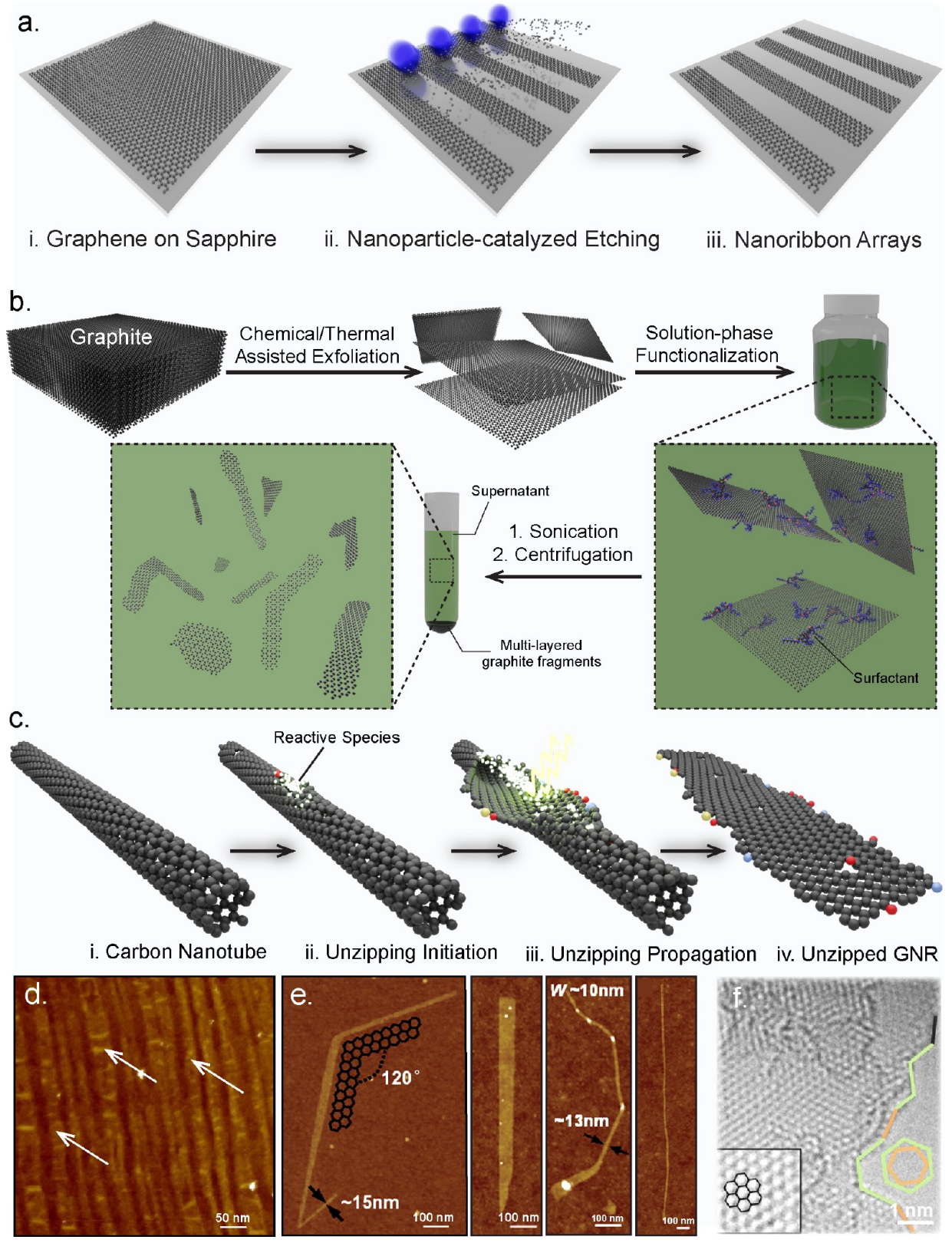

Figure 4. GNR fabrication *via* top-down nanocutting techniques. (a) Creation of GNR arrays using nanoparticle-catalyzed etching of graphene. (b) Solution-phase sonochemical unzipping of graphite to produce GNRs and graphene crystals of different shapes. (c) Conceptual schematic of unzipping CNTs to produce GNRs. Unzipping can be initiated by catalytic nanoparticles, oxidizing agents, or plasma. (d) Atomic force microscopy (AFM) image of arrays of GNRs created by nanoparticle-assisted etching of graphene. GNRs are indicated by white arrows. Adapted with permission from ref 126. Copyright 2014 Elsevier. (e) GNRs of varied shapes and widths obtained by sonochemical unzipping of graphite. Adapted with permission from ref 90. Copyright 2008 AAAS. (f) Transmission electron microscopy (TEM) image of GNRs produced by unzipping CNTs *via* electrochemical oxidation. The GNR edge structure is highlighted in green and orange. Reproduced with permission under a Creative Commons CC-BY 4.0 license from ref 136. Copyright 2016 Springer Nature.

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GNRs facilitate integration on flexible platforms for wearable and stretchable applications.[76,77] While armchair GNRs are promising for conventional electronics, zigzag, heterostructured, and doped GNRs, due to their exotic magnetic and spin-polarized edge states, could enable graphene-based spintronic devices in memory, logic, neuromorphic, and quantum computing.[48,53,78−82] Considering the increasing shift of industry toward system scaling, *i.e.*, heterogeneous integration of varied functionalities on a single chip,[83] GNRs may meet the performance requirements of diverse logic, non-Von Neuman, and beyond-CMOS technologies.[84,85] Moreover, the utility of GNRs is not limited solely as a channel in the front-end-of-line (FEOL). In fact, a key issue throttling the performance of contemporary integrated circuits is the interconnect delay ($\tau = RC$) in the back-end-of-line (BEOL) due to enhanced resistivity and electromigration of Cu at sub-20 nm widths, and this issue has stalled interconnect scaling in recent years.[86] Atomically thin GNRs exhibit not only an order of magnitude higher current carrying capacity ($\sim 10^8$ A cm^{-2} versus 10^7 A cm^{-2} for Cu)[23,26,87] but also much higher resistance to electromigration (*i.e.*, longer time-to-failure)[23] and thermal conductivity (~2000 versus 400 W m^{-1} K^{-1} for Cu),[88] making them prospective successors to Cu in BEOL.

Despite such promising theoretical and experimental data,[36,37,56,59,89−91] several significant materials science challenges need to be overcome for GNRs to be adapted into mainstream electronics.[92,93] Analogous to the hurdles that have challenged the field of CNT electronics for more than two decades,[10,94,95] these can be classified as follows:

(1) *Production challenges*: the scalable production of monodisperse assemblies of narrow GNRs with controlled crystallographic orientation (*i.e.*, armchair, zigzag, or chiral) and smooth edge structures and their rational placement and alignment on arbitrary substrates with nanometer precision.

(2) *Integration and device engineering challenges*: the integration of GNRs into devices with small contact resistances at metal−GNR interfaces, uniform dielectric environments, and encapsulation.

In this Review, we present a brief overview of the recent advances in GNR fabrication and electronics, challenges that must be overcome, and a vision for the field going forward.

CURRENT STATE OF GRAPHENE NANORIBBON RESEARCH AND CHALLENGES

Production. *Lithography.* The fabrication of GNRs has significantly evolved over the past 12 years. Initial attempts at producing GNRs involved top-down lithographic patterning of continuous graphene sheets using electron-beam lithography in conjunction with reactive-ion etching.[62,96] Electron-beam lithography is conceptually simple and potentially scalable and yields GNRs with precise placement, allowing for the wafer-scale integration of GNRs into devices (Figure 3a). Additionally, arrays of nanoribbons with well-defined periodicity (*i.e.*, identical pitch), which will be paramount in multichannel FETs, can be easily fabricated by this approach.[97,98] However, GNRs obtained by electron-beam lithography are generally more than 10 nm wide, which is insufficient to induce a technologically relevant band gap $\gg k_BT$ of 25 meV at room temperature.[35] Even narrower GNRs have been reported *via* exploratory lithographic techniques such as helium ion beam lithography,[99−101] meniscus mask lithography,[102] block copolymer lithography,[97,98,103] graphene edge lithography,[104] and scanning tunneling microscopy (STM) lithography.[105] However, these nonconventional lithographic techniques are either unscalable or unexplored for high-volume manufacturing.[106] Another approach to achieve narrower GNRs *via* lithography is to add a secondary post-lithography gas-phase or plasma-etching step.[107−109] However, when fabrication of GNRs with sub-5 nm widths is attempted, these etching approaches frequently result in discontinuous GNRs due to pre-existing non-uniformities along the GNR edges.[107,110]

In general, lithographic patterning lacks atomic resolution, which causes a mixture of armchair edges, zigzag edges, and dangling bonds; results in high line-edge roughness; and functionalizes the GNR edges (Figure 3a, step vi; and Figure 3b). Such inhomogeneities and disorder lead to severely degraded carrier mobility and thermal conductivity, Coulomb blockade, and high off-currents—with effects that become increasingly detrimental with decreasing GNR width.[34,112−118] For example, the room-temperature carrier mobility of 12 nm wide, lithographically patterned GNRs of <10^2 cm^2 V^{-1} s^{-1} is over 2 orders of magnitude lower than the theoretically predicted value of ~10^4 cm^2 V^{-1} s^{-1}.[119] Similarly, the largest on/off current ratio (I_{on}/I_{off}) measured in ~5 nm wide, lithographically patterned GNRs at room-temperature is <200 [whereas $I_{on}/I_{off} > 5 \times 10^3$ should be possible based on theoretical predictions of a relationship between band gap and I_{on}/I_{off} (see logic figures of merit in the Integration and Device Engineering section, below) and experimental results (see the section on Bottom-up Organic Synthesis, below)], limiting the potential applications of GNRs fabricated by these techniques.[120−124] Some recent device studies have realized high on-state conductance in lithographically patterned ~10 nm wide GNRs, albeit with comparatively low I_{on}/I_{off}.[125]

Top-Down Cutting of Graphene, Graphite, or Carbon Nanotubes (CNTs). Besides lithography, GNRs can be derived from several other allotropes of carbon. Three major approaches falling under this umbrella are (1) catalytic nanocutting of graphene (Figure 4a,d),[126−128] (2) top-down sonochemical unzipping of graphite (Figure 4b,e),[37,90,129] and (3) solution- or plasma-mediated unzipping of CNTs[130−135] (Figure 4c,f). In approach 1, GNRs are derived by metal nanoparticle-assisted etching of graphene. Generally, this technique yields zigzag-edged GNRs since nanoparticles predominantly etch along zigzag directions of graphene.

While it is possible to fabricate dense GNR arrays using this technique, control over GNR width, placement, array pitch, and alignment remains a formidable challenge due to lack of control over the trajectory along which nanoparticles etch. In approach 2, GNRs are obtained *via* gas-phase exfoliation of bulk graphite crystals followed by sonication-assisted solution-phase rupture of graphene sheets into shapes with varied morphology. Analogous to approach 2, in approach 3, GNRs can be derived by unrolling CNTs along their length, commonly accomplished *via* plasma treatment, oxidative reagents, or electrochemistry. Although, in principle, both approaches 2 and 3 can be scaled for bulk production of GNRs, challenges remain pertaining to low-yield, width-polydispersity, chirality control, and placement- and alignment-control. An additional challenge with these is also the potential for defect creation and/or inadvertent functionalization during plasma treatment and sonication, which need to be studied in more detail.

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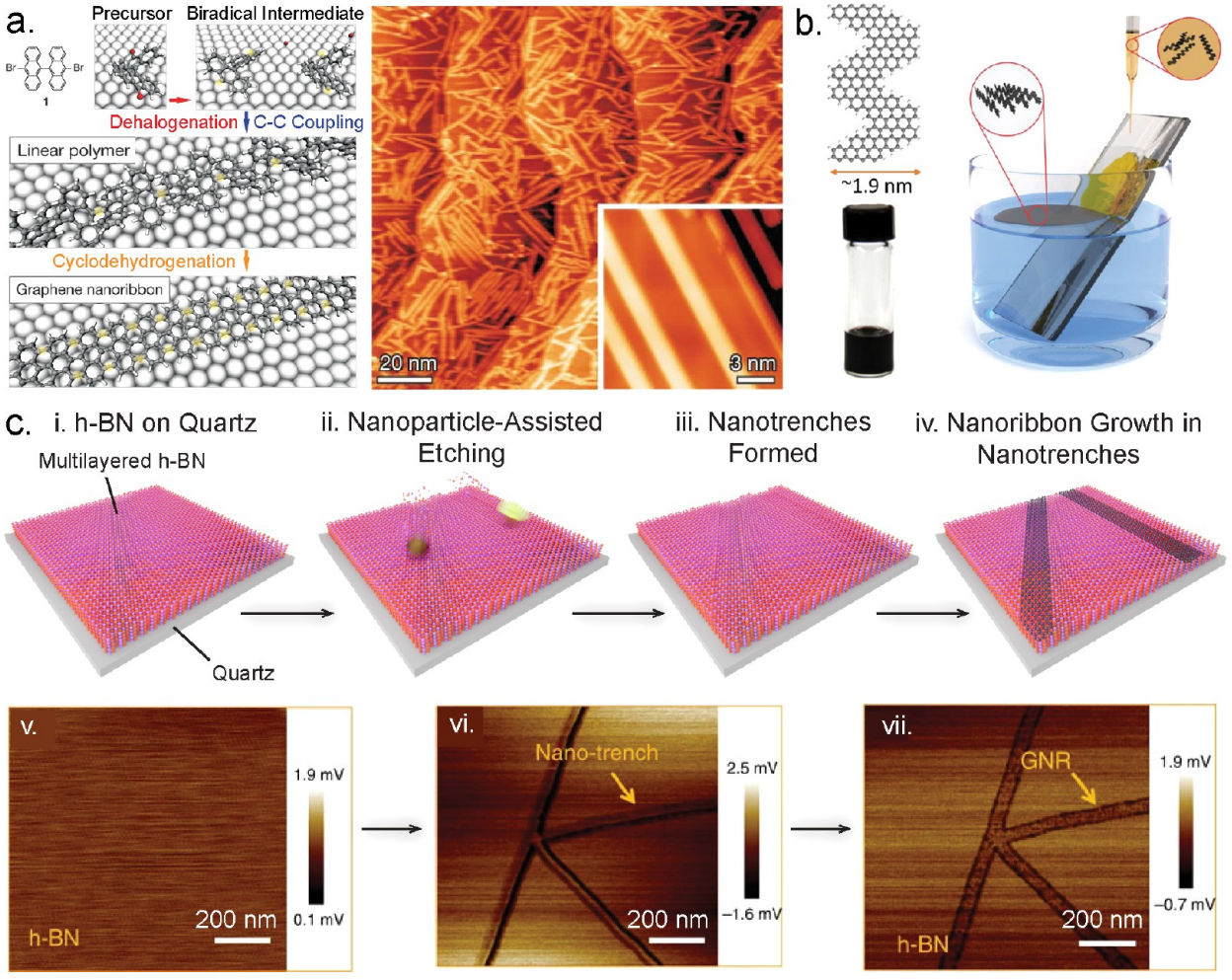

Figure 5. Bottom-up production of GNRs *via* organic synthesis and lateral heteroepitaxy. (a) On-surface polymerization of 10,10′-dibromo-9,9′-bianthryl and subsequent cyclodehydrogenation to synthesize n = 7, armchair GNRs. STM shows polymerized GNRs on Au(111) terraces. Reproduced with permission from ref 171. Copyright 2016 Springer Nature. (b) Solution-phase polymerization to produce chevron GNRs and interfacial self-assembly to obtain uniform thin films of GNRs. Reproduced with permission from ref 194. Copyright 2017 American Chemical Society. (c, i–iv) Schematic of GNR synthesis in etched h-BN trenches; and (v-vii) corresponding AFM friction images demonstrating trench fabrication and GNR growth. Reproduced with permission under a Creative Commons CC-BY 4.0 license from ref 196. Copyright 2017 Springer Nature.

Despite these challenges, a major benefit of some of these methods is that they can yield GNRs with lower line edge roughness and therefore demonstrate better electronic performance than lithographically defined GNRs.[137] For instance, GNRs derived from sonochemical unzipping of graphite in refs 37 and 90 demonstrated room-temperature carrier mobility of 200 $cm^2\ V^{-1}\ s^{-1}$ and an impressive I_{on} = 2000 $\mu A\ \mu m^{-1}$ at I_{on}/I_{off} of 10^6–10^7. While some of the challenges mentioned above might make it difficult for GNRs produced by these techniques to be incorporated in high-performance semiconductor electronics, there are several other applications wherein these GNRs might play an important complementary role.[96,138] For instance, self-assembled GNR films achieved *via* unzipped CNTs are promising for low-cost electronics such as gas sensors and thin-film transistors.[136]

Bottom-Up Organic Synthesis. The critical need to achieve narrow GNRs with smooth edges has motivated the exploration of bottom-up synthetic routes,[139] wherein the idea is to couple or polymerize tailored organic monomers in order to synthesize atomically precise GNRs on the surface and in solution. For example, one common organic synthesis route involves aryl–aryl coupling of 10,10-dibromo-9,9 bianthracene (DBBA) on a metallic surface (*e.g.*, Ag, Au, or Cu) followed by cyclodehydrogenation and graphitization to yield atomically precise GNRs (Figure 5a).[140,141] The promise of these techniques lies in the ability to achieve sub-2 nm widths with atomic precision and the ability to tune the GNR structure and edge topology and, therefore, properties by rational choice of the monomeric building blocks. Consequently, armchair,[39,142–146] zigzag,[147] chiral,[148,149] topological,[150–154] edge-functionalized,[155–158] doped,[29,159–161] and heterostructured[162–167] GNRs and several others with intricate edge topologies (*e.g.*, chevron,[168] cove,[169] fjord,[170] *etc.*) have been synthesized. While the surface-mediated organic synthesis of GNRs was initially demonstrated in ultrahigh vacuum (UHV),[171] it has now been reproduced at ambient pressures by sublimating or drop-casting precursors followed by chemical vapor deposition or thermal annealing, improving the facility and scalability of this technique for the production of atomically flat GNRs.[93,172,173] FETs fabricated from GNRs grown by bottom-up organic synthesis have demonstrated promising performance, yielding $I_{on} \sim 1\ \mu A$ at $I_{on}/I_{off} \sim 10^5$.[59]

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Additionally, gram quantities of GNRs have been produced by various solution-phase approaches.[174,175] Conceptually similar to surface-mediated polymerization, here, polyphenylene precursors (commonly prepared by coupling similar or dissimilar aromatic monomers) are polymerized and graphitized to yield GNRs in solution (Figure 5b).[175,176] Since such GNR dispersions can be dip-coated or drop-cast on arbitrary surfaces, this versatile technique could be used for facile fabrication of thin-film transistors, biosensors, organic photovoltaic devices, composites, and coatings.[177−183]

There are, however, a few challenges. Most GNRs synthesized by surface-mediated organic synthesis are rather short in length (<50 nm) due to interruption of the polymerization process by surface defects and step edges. The short lengths make it challenging to contact the GNRs with metal electrodes for their integration into devices and especially challenging to form low-resistance contacts due to the resulting short length of the GNR−metal contacts.[184] With this said, encouraging advances in increasing GNR length to >100 nm have been recently reported in some instances by engineering surface step-topology and reconstruction.[185,186] A recent report has also demonstrated that some edge roughness might be present in some of these GNRs due to missing benzene rings at edges, degrading I_{on} by up to an order of magnitude—necessitating an even more careful choice of precursors.[187] Additionally, organic synthesis has been primarily confined to metallic surfaces, although practical realization of GNR-based electronics requires direct synthesis on or high-yield, residue-free transfer to CMOS-compatible substrates. Furthermore, so far, most surface-mediated approaches yield randomly oriented GNRs with relatively poor control over placement and density. In contrast, aligned assemblies of GNRs with rational placement are needed for most semiconductor applications.[188,189] Aligned GNR synthesis on stepped Au surfaces, for instance, is an impressive step in this direction.[190] Another challenge lies in synthesizing super-1.5 nm wide GNRs, which is primarily due to difficulties in synthesizing and processing large monomers. However, wider GNRs with smaller band gaps could be advantageous for forming low-resistance contacts in GNR FETs and for a broad range of high-conductance applications.

Solution-mediated polymerization offers some advantages over surface-mediated polymerization, while also introducing additional challenges. For example, GNRs with lengths >500 nm have been demonstrated, and improved control over length-polydispersity has recently been attained.[170,175] Moreover, liquid-phase processability has enabled the uniform deposition of conducting GNR films, which may be useful for thin-film applications.[174,191] However, GNRs derived by solution-phase synthesis can be challenged by agglomeration, and in some cases—similar to CNTs—it has proven challenging to reliably disaggregate individual GNRs or deposit their aligned assemblies on arbitrary substrates, which is crucial for FETs.[192] Some studies have reported improved dispersibility in solution *via* introduction of functional substituents (*e.g.*, polymer or bulky 3D chains) on the GNR edges, and alignment within films has been achieved *via* self-assembly approaches. However, the electronic characteristics of devices fabricated from such films are decreased by GNR−GNR screening effects, which reduce electrostatic control over the channel and lead to high inter-GNR resistance, leading to degraded performance of long-channel devices in which charge carriers must percolate between GNRs within the film.[193,194] Experimentally, the impact of edge functionalization on intrinsic GNR electronic properties is not well-understood, even though theoretically it is believed that in some cases edge functionalization could profoundly impact band structure, doping, and transport properties.[195]

Lateral Heteroepitaxy in Hexagonal Boron Nitride (h-BN) Nanotrenches. GNRs laterally embedded within sheets of hexagonal boron nitride (h-BN) have been synthesized by two approaches: (1) chemical vapor deposition (CVD) within trenches of h-BN created by metal nanoparticle-assisted etching[196,197] and (2) alternating in-plane heteroepitaxy of graphene and h-BN.[198] Graphene and h-BN have the same crystal structure and similar lattice constants; therefore, lateral GNR−h-BN heterostructures provide a promising avenue for passivating GNR edges, thereby preventing inadvertent doping or edge functionalization (Figure 5c). Notably, GNRs fabricated in h-BN trenches have exhibited the highest field-effect mobilities ($\mu \approx 1500$ cm^2 V^{-1} s^{-1}) reported for sub-10 nm wide GNRs in the literature, while simultaneously exhibiting impressive $I_{on}/I_{off} \sim 10^5$. These high-performance device metrics are possibly due to passivation of the GNR edges by h-BN or shielding of the SiO_2 gate dielectric by underlying h-BN concurrently transferred with the GNRs.[196,197,199] For example, related work has demonstrated improved stability of graphene quantum dots embedded in h-BN, which was attributed to edge passivation,[200] and graphene on h-BN exhibits an increase in mobility compared to graphene on SiO_2 (due to the smooth h-BN surface with low trap density and reduced scattering).[201] Therefore, it is conceivable that these two factors are important to realize superior GNR electronic behaviors in FETs.[196]

Templated Synthesis. i. CVD on Patterned Templates of Nickel. CVD on lithographically patterned metallic templates on dielectrics (*e.g.*, Ni nanobars on SiO_2) has also been explored to achieve site-specific GNR synthesis. In this process, the metallic template is removed after GNR synthesis by sublimation or wet etching, yielding GNRs directly on a dielectric.[202,203] However, this strategy has not yet yielded sub-10 nm wide GNRs with well-defined edges due to the resolution limits of the lithography that is used to pattern the metallic templates and due to the instability of sub-10 nm metal stripes at the high temperature required for GNR growth. Moreover, CVD on Ni yields multilayered GNRs with mixed edge-chirality. Consequently, GNRs produced on Ni templates have poor I_{on}/I_{off}, which limits their utility in most FET applications. The presence of residual metal might further inhibit integration in semiconductor processing tools, which is also a challenge in other production methods that utilize a metal surface.[188,204] Additional research is required to elucidate the GNR edge structure and reduce the GNR width.

ii. Synthesis on SiC Nanofacets. The synthetic techniques discussed above have a common limitation; *i.e.*, none facilitate bottom-up growth of GNRs directly on a technologically relevant platform—a key factor for industry to adopt a new materials technology, as transfer techniques present scaling, yield, and cleanliness challenges. Epitaxial growth on SiC is a metal- and transfer-free, bottom-up approach for synthesizing GNRs that avoids these challenges.[72] In this process, SiC sidewall nanofacets are first generated by annealing lithographically patterned SiC trenches at ∼1200 °C. Then, the nanofacets undergo a second anneal at a higher temperature of ∼1450 °C in an appropriate Si vapor pressure environment, which causes selective controlled sublimation of Si atoms,

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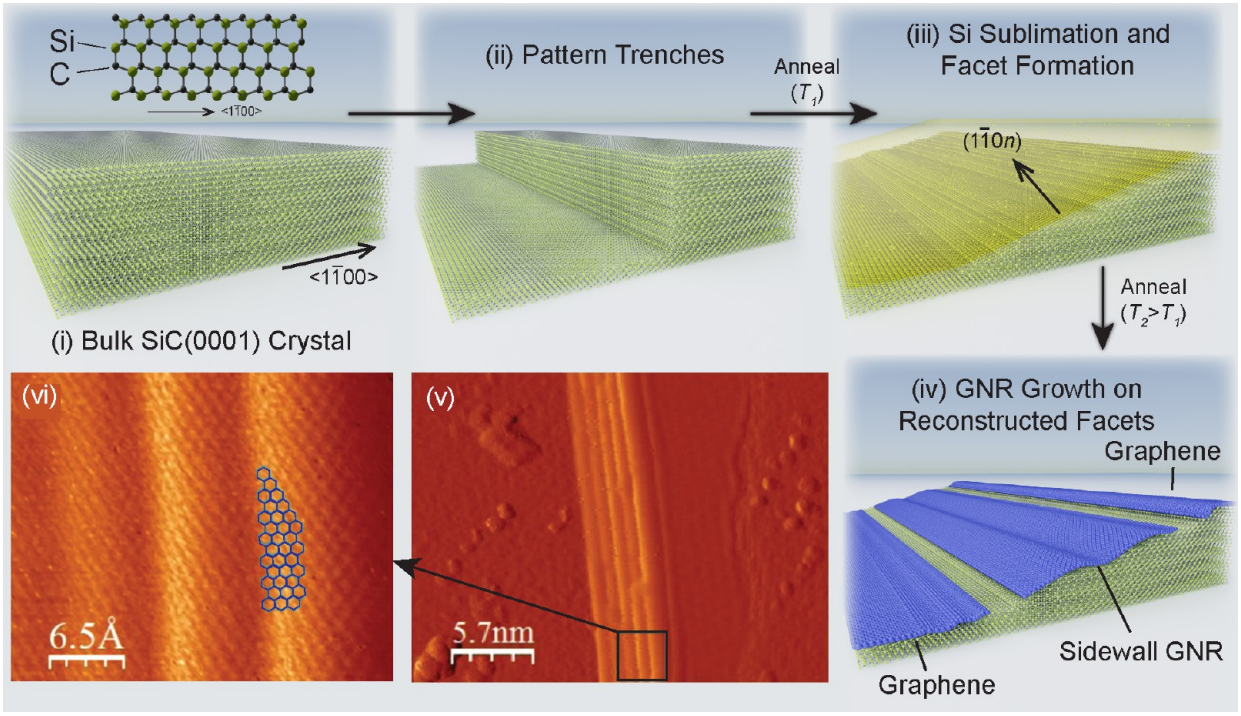

Figure 6. Bottom-up synthesis of GNRs on SiC. (i–iv) Schematic of synthesis of GNRs on SiC (1$\bar{1}$0n) nanofacets formed by annealing-induced reconstruction of lithographically patterned trenches. STM images of miniribbons formed on SiC nanofacets are shown at different scales in panels v and vi, wherein the graphene lattice is distinguished. Reproduced with permission from ref 208. Copyright 2015 American Chemical Society.

leaving C atoms that self-organize into GNRs on the nanofacets (Figure 6i–iv). Besides allowing for improved control over GNR placement, this strategy allows facet-specific tuning of GNR chirality; *e.g.*, SiC(0001) trenches parallel to ⟨1$\bar{1}$00⟩ yield GNRs with zigzag edges whereas those parallel to ⟨11$\bar{2}$0⟩ yield GNRs with armchair edges.[205] Furthermore, the specific SiC polytype (*i.e.*, 4*H*-SiC versus 6*H*-SiC) profoundly influences the structural and electrical properties of the resulting sidewall GNRs due to intricate differences in GNR–substrate interactions, termination, and facet morphology.[206,207] For instance, trenches that yield armchair GNRs on 4*H*-SiC (*i.e.*, parallel to ⟨11$\bar{2}$0⟩) predominantly evolve into a single (1$\bar{1}$07) facet upon annealing, bordered by (1$\bar{1}$05) minifacets at the top and bottom terraces,[208] whereas trenches that yield zigzag GNRs on 6*H*-SiC (*i.e.*, parallel to ⟨1$\bar{1}$00⟩) evolve into an array of 2–3 nm wide (11$\bar{2}$2) minifacets—yielding decoupled GNRs (termed miniribbons) with different widths and densities. Similarly, whereas zigzag GNRs on 6*H*-SiC exhibit ballistic transport, zigzag GNRs on 4*H*-SiC are diffusive conductors (*i.e.*, GNR conductance inversely correlates with length).[206] Since the GNRs synthesized on such nanofacets are typically more than 20 nm wide, they are semimetallic. However, in the miniribbon portion of GNRs, signatures of electronic confinement are observed in angle-resolved photoemission spectroscopy (ARPES), indicating the presence of a local band gap. For example, in the case of armchair GNRs synthesized on 4*H*-SiC, an appreciable band gap (>0.5 eV) is observed in regions of the GNR draped over (1$\bar{1}$05) minifacets due to the binding of the edge of the GNR to the buffer layer graphene, whereas the central region of the GNR draped over the central (1$\bar{1}$07) facet exhibits room-temperature ballistic transport with no significant band gap.[208,209] Consequently, it might be possible to realize dense FET arrays wherein the semimetallic portion of the GNRs is utilized as source–drain contacts to the semiconducting regions of the GNRs.[72,210] Charge transport through the semiconducting regions, however, has not yet been measured.

Although GNRs greater than 20 nm wide could be used as interconnects,[208] their BEOL integration would be challenging due to the high thermal budget of synthesis.[211] To utilize GNRs grown on SiC nanofacets as a semiconducting FET channel material, it will be necessary to either (i) reduce the overall GNR width to less than 10 nm to open an appreciable band gap in the semimetallic GNR region or (ii) learn how to exclusively synthesize miniribbons isolated from the semimetallic regions. Promising strides have been made to reduce the GNR width by tuning the depth of the lithographically patterned trenches in SiC to yield narrower sidewall facets[212] and by conducting synthesis on vicinal SiC (0001) surfaces, which naturally contain narrow, well-aligned facets.[213] These approaches can yield arrays of ∼10 nm wide GNRs with armchair edges; however, FETs from these GNRs have not yet been demonstrated. A combination of substrate miscut and etching could be explored to fabricate narrower facets. One challenge is that large miscuts in SiC are known to facilitate the growth of few-layered graphene, leading to variable device characteristics.[214,215] Furthermore, the presence of natural steps on SiC(0001) is known to facilitate inadvertent GNR growth, reducing the control over their placement, and elimination of such steps requires additional high-temperature processing.[216]

CVD on Germanium. Initially demonstrated by our group in 2015, CVD on Ge(001) has emerged as another attractive bottom-up technique to synthesize GNRs directly on a technologically relevant platform.[70] Catalytic decomposition

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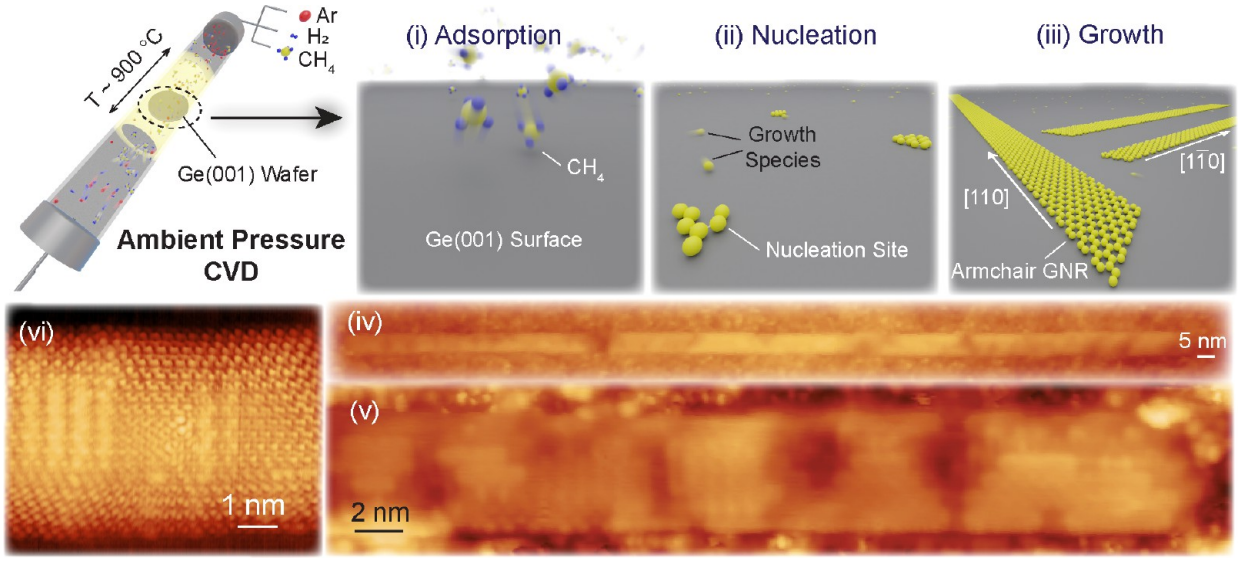

Figure 7. Synthesis of GNRs on Ge(001). (i–iii) Schematic of CVD of armchair GNRs on Ge(001) at ambient pressure. (iv–vi) STM images at different scales, showing GNRs synthesized on Ge(001) with high-fidelity edges. Reproduced with permission from ref 222. Copyright 2019 American Chemical Society.

of a hydrocarbon precursor (*e.g.*, methane) at high temperatures on the Ge(001) surface causes nucleation and growth of graphene.[217] At slow growth rates (*i.e.*, low supersaturation of hydrocarbon precursors), the graphene evolves anisotropically, yielding self-defining GNRs that are oriented along Ge⟨110⟩ and possess long segments of smooth armchair edges (Figure 7). The resulting GNRs have a semiconducting band structure and competitive charge transport properties, simultaneously exhibiting $I_{on}/I_{off} \sim 2 \times 10^4$ and $I_{on} \sim 0.5$ μA at a relatively low source-drain bias of 0.1 V.[89,218] Using this approach, GNRs with widths down to 1.7 nm have been demonstrated, and the width can be tuned simply by varying growth time and/or precursor concentration during CVD.[219] Although spontaneous nucleation yields GNRs that are polydisperse and randomly placed on the surface, progress toward overcoming these challenges has recently been made by initiating synthesis from deterministically placed sub-5 nm graphene nanoseeds on the Ge(001) surface, which have resulted in substantial improvements in dimensional monodispersity and unidirectional alignment.[71,220] It has also been demonstrated that growth of unidirectionally aligned GNRs can be achieved on vicinal Ge(001).[73,221] Furthermore, these breakthroughs can be extended to CMOS-compatible Ge/Si(001), which is a promising approach toward front-end-of-line (FEOL) integration of GNRs on a Si platform for both logic and analog/RF applications.[222]

Notwithstanding these promising results, there are challenges. Synthesis of GNRs *via* CVD requires high temperatures (~900 °C) and slow growth rates (length growth rate ~ 40 nm h^{-1}). Currently, atomic-scale control over GNR widths and edge structures is lacking; this control is paramount for precisely engineered band gaps, as the band gap fluctuates with each additional atom along the width in the sub-5 nm width regime (Figure 1b). Seed-initiated growth also needs to be improved to further reduce width-polydispersity, while still achieving high yield and maintaining control over placement and alignment. Other potential concerns are the nanofaceting and roughening of the Ge surface during the CVD growth,[223,224] which might degrade GNR carrier mobilities in applications utilizing the GNRs directly on the Ge surface.[225] Moreover, currently, the fabrication of GNR devices requires transfer to a dielectric surface (*e.g.*, HfO_2 or SiO_2) due to doping of the Ge during CVD, whereas fabrication of GNR devices directly on Ge would be much more suitable for CMOS integration.[226]

Integration and Device Engineering. *Key Competitive Metrics/Figures of Merit (FOMs) for Applications. i. Logic.* While the GNR research community has made impressive strides in overcoming synthesis bottlenecks, GNRs still need to demonstrate power–performance–area–cost (PPAC, *i.e.*, lower power and higher performance for a given footprint at reduced cost), reliability, and yield metrics that are competitive with current state-of-the-art Si FinFET and SOI technologies to be viable contenders in high-volume commercialization.[227,228] Primarily, GNR FETs should be able to achieve higher performance and/or lower stand-by power, where the former is related to the maximum on-state current (I_{on}), and the latter is in part determined by the ratio of transistor drain currents in "on" and "off" states (I_{on}/I_{off}). Generally, for logic applications, I_{on}/I_{off} must exceed 10^4—translating to a channel band gap (E_g) of at least 0.4 eV [$(I_{on}/I_{off} \approx \exp(E_g/2k_BT))$, where k_B is the Boltzmann constant and T is temperature].[229] For high-performance logic (*e.g.*, personal computers, data centers, high-end mobile, graphics processing units (GPUs), *etc.*), it is critical to have a large I_{on} to minimize delay (or maximize the transistor switching speed, where switching delay $\tau = CV_{DD}/I_{on}$, in which V_{DD} is the supply voltage, and C is the gate capacitance),[230] whereas for low-power logic (*e.g.*, cell phones, tablets, Internet of things (IoT) devices, *etc.*), it is paramount to minimize the static power consumption by minimizing I_{off}.[84,231]

Until a few years ago, when FET channels were several tens of nanometers long ($L_{ch} > 20$ nm), a channel material with high charge carrier mobility (μ) (*e.g.*, with long scattering length and low carrier effective mass (m_{eff})) was preferred to achieve high I_{on}.[232] This is because carrier drift velocity is directly proportional to μ ($v_{drift} = \mu E$, where E is the applied electric field), and faster carriers yield larger I_{on} (current, $I = q$

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Table 1. Summary of Key Metrics for Different Applications[a]

Application	Relevant metric	Current state-of-the-art technology	Theoretically predicted or simulated values for GNRs
Logic	On-state current (I_{on})	1.8 mA μm^{-1} (10 nm Si FinFET)[236] at 0.7 V	1−2.5 mA μm^{-1} (depending on pitch)[249,250] at 0.5 V
	On/off ratio (I_{on}/I_{off})	10^4−10^7	10^6 (w_{GNR} = 2.1 nm)[249,250]
	Subthreshold swing (SS)	68 mV dec^{-1} (5 nm Si FinFET)[86]	68 mV dec^{-1} (n = 16 armchair GNR FET)[62]
	Drain-induced barrier lowering (DIBL)	35 mV V^{-1} (5 nm Si FinFET)[86]	62 mV V^{-1} (n = 16 armchair GNR FET)[62]
Radio-frequency	Transconductance (g_m)	3 mS μm^{-1} (14 nm Si FinFET)[240]	9 mS μm^{-1} (w_{GNR} = 1.1 nm)[253]
	Cut-off frequency (f_T)	314 GHz (14 nm Si FinFET),[240] 610 GHz (InP HEMT)[242]	∼1 THz (n = 16 armchair GNR FET)[62]
	Maximum oscillation frequency (f_{max})	299 GHz (22 nm FDSOI),[241] 1.5 THz (InP HEMT)[242]	∼1 THz (n = 16 armchair GNR FET)[62]
Thin-film electronics	Mobility (μ)	10 cm^2 V^{-1} s^{-1} (IGZO)	≥100 cm^2 V^{-1} s^{-1}
Interconnects	Maximum current density	10^7 A cm^{-2} (copper)[87]	10^8 A cm^{-2} (w_{GNR} = 16 nm)[26]
	Thermal conductivity	385 W m^{-1} K^{-1} (copper)[87]	2000 W m^{-1} K^{-1} (1.5 nm wide ZGNR)[88]

[a]Theoretically predicted values for GNRs are compared with current state-of-the-art technologies. (FDSOI = fully depleted silicon-on-insulator).

$\times A \times v_{drift}$, where q is the carrier charge, and A is the cross-sectional area of the conduction channel). However, in the short-channel regime, typical of contemporary ultrascaled FETs (L_{ch} < 20 nm), the effect of μ on I_{on} is less important due to quasiballistic or ballistic transport across the channel and the relative predominance of parasitic capacitances and resistances.[233] For L_{ch} < 10 nm, channel materials with higher m_{eff} are needed to suppress quantum-mechanical source-to-drain tunneling.[234,235]

Other relevant metrics are (1) subthreshold swing (SS), which characterizes the swiftness with which a transistor can turn on or off, and (2) drain-induced barrier lowering (DIBL), which is related to the gate's electrostatic control over the channel. It is important to minimize these parameters to ensure continuous downscaling of V_{DD} while minimizing I_{off}. As a benchmark, industry-leading 5 nm node Si FinFETs exhibit $G_{on} \approx 1.5$−2 mS μm^{-1}, $I_{on}/I_{off} \approx 10^5$− 10^7, SS ≈ 68 mV dec^{-1} (Boltzmann limit being 60 mV dec^{-1} at room temperature), and DIBL ≈ 35 mV V^{-1} at $V_{DD} \approx 0.75$ V.[86,236] The actual parameters might differ depending on the specific application (*e.g.*, high performance or low power).

ii. Analog/Radio Frequency (RF). For analog applications, such as low-power wireless receivers and low-noise amplifiers, two important figures of merit are transconductance (g_m) and intrinsic gain (or self-gain) (G_{int}), which determine the maximum speed and/or gain that a transistor can achieve. In RF applications, relevant metrics are cutoff frequency (f_T) and maximum oscillation frequency (f_{max}), which correspond to the frequency at which the small signal current gain and power gain of the transistor, respectively, drop to 0 dB and are indicative of the maximum possible operational frequency of the transistor.[237] Since both g_m and f_T are directly proportional to μ, a channel with high μ is advantageous. However, in high-performance RF transistors, which typically have short channels (L_{ch} < 30 nm), electron velocity saturates; therefore, μ is no longer a useful metric, and instead, device performance is determined by the saturation velocity (v_{sat}) and m_{eff}.[84] Besides a high μ or v_{sat}, it is also critical to achieve satisfactory drain saturation to maximize G_{int} and f_{max}. This saturation necessitates a semiconducting channel with a band gap > 0.17 eV.[238,239] Furthermore, other critical parameters such as the noise figure (*i.e.*, the noise that the RF device adds to the signal), impedance mismatch, and linearity (*i.e.*, how linear is the change in output with respect to change in input) must also be considered. As a benchmark, Si-based devices (FinFET/SOI with $L_g \approx$ 20−30 nm) can exhibit f_T and $f_{max} \approx$ 300−400 GHz, $G_{int} \approx 40$, and $g_m \approx 3$ mS μm^{-1}.[240,241] Meanwhile at similar gate lengths, HEMTs of III−V materials such as InP have attained f_T and f_{max} values approaching 1 THz with $g_m \approx 3$ mS μm^{-1}.[242] Noteworthy is the fact that RF circuits are less complex than logic, and therefore, the barrier for commercial adoption of new materials may be lower than in logic.

iii. Thin-Film/Flexible Electronics. GNRs could also face fewer obstacles to commercialization in thin-film electronics (*e.g.*, FETs in the backplane of displays, chemical and biological sensors, and printed, flexible, stretchable, and bioelectronics) due to the much lower process complexity and performance required for these applications.[181] Although thin-film electronics encompass a wide range of applications, generally a high μ and I_{on}/I_{off} are desirable.[243,244] For instance, current thin-film transistors in displays, which are based on indium gallium zinc oxide (IGZO), have μ of around 10 cm^2 V^{-1} s^{-1} and $I_{on}/I_{off} > 10^8$ in commercial implementations (with μ up to 70 cm^2 V^{-1} s^{-1} in the laboratory).[245] Generally, thin-film electronics applications require $\mu \sim$ 0.1−100 cm^2 V^{-1} s^{-1} and large $I_{on}/I_{off} \sim 10^6$ to minimize power dissipation.[246−248]

Benchmarking Theoretical GNR Performance and Current State-of-the-Art Experimental Performance. Keeping these benchmarks in mind, it is worth comparing the predicted performance of GNRs in logic, RF, and thin-film applications to the performance of existing state-of-the-art technologies. (See Table 1.) Theoretical calculations predict that GNR FETs with top gates can achieve high $I_{on}/I_{off} > 10^6$ and I_{on} in the range 1−2.5 mA μm^{-1} (depending on pitch), meeting or exceeding the 2030 ITRS target of I_{on} = 1.5 mA μm^{-1} for low-power logic at L_g of 10 nm.[249−251] Moreover, the atomic thickness and narrow width (≈2 nm) of the GNR channel afford improved gate electrostatics and are predicted to yield SS of 68 mV dec^{-1} and DIBL of 62 mV V^{-1} at $L_g \approx$ 20 nm, better than SOI MOSFETs and comparable to Si FinMOSFETs scaled to a similar L_g.[62,236] A concern, however, arises with the suitability of GNRs for aggressively scaled logic FETs at sub-10 nm channel lengths due to relatively small effective mass (*e.g.*, m_{eff} for 1 nm wide armchair GNR in the $3p$ + 1 family is ∼ $0.2m_o$ versus $0.29m_o$ for Si), which has been predicted to lead to source-to-drain tunneling, although such tunneling effects in GNRs have not been studied exper-

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imentally.[63,252] In RF applications, GNRs are predicted to exhibit $g_m \approx 9$ mS μm^{-1} due to their high intrinsic μ, v_{sat}, and semiconducting band structure, yielding f_T and f_{max} values of 1−2 THz.[253] While the projected RF performance is comparable to III−V's, GNR FETs (like carbon nanotube FETs) are expected to offer superior linearity and more facile routes to integration onto Si without lattice-matching constraints.[254] Furthermore, assuming longer and/or covalently interconnected GNRs can be made, they should be able to easily meet the requirements of thin-film technologies, owing to the large predicted μ ($\geq$100 cm^{-2} V^{-1} s^{-1}) and I_{on} ($\geq$1 mA μm^{-1}) at $L_{ch} > 1$ μm—the typical L_{ch} of modern thin-film devices.[37,90,255]

However, experimentally it has been challenging to realize GNR FET metrics close to these projected values (Figure 8).

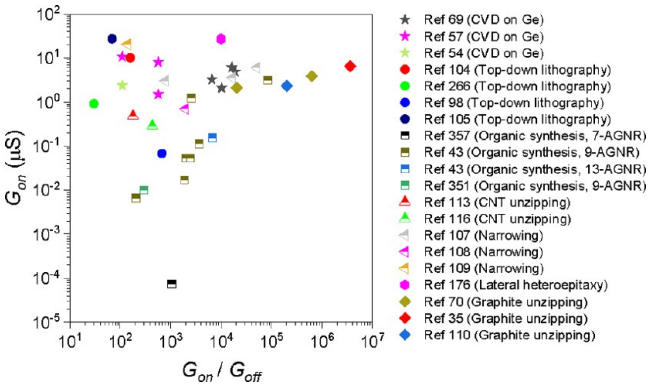

Figure 8. Plot of on-state conductance *versus* on/off conductance ratio reported for GNR FETs produced by different techniques. Data are partly adapted from ref 73.

For instance, GNR FETs with acceptable I_{on}/I_{off} (*i.e.*, $>10^4$) fabricated from chemo-mechanical cutting of graphite have exhibited an $I_{on} = 4$ μA (or $G_{on} = 8$ μS or $G_{on}/w = 1$ mS μm^{-1}) at L_{ch} of 236 nm,[73] which is ~10 times lower than the quantum conductance limit of 77 μS ($2e^2/h$).[256] In this technique, SS and g_m have also been subpar, with the best values reaching only 210 mV dec^{-1} and 0.9 mS μm^{-1}, respectively.[37] GNRs fabricated by lateral heteroepitaxy in h-BN trenches have exhibited better performance in terms of on-current. In this case, ~5 nm wide GNRs exhibit a $G_{on} = 27$ μS (or 5.4 mS μm^{-1}) and I_{on}/I_{off} of 10^4 at L_{ch} of 300 nm.[196] It is possible that passivating the edges of GNRs—one distinguishing feature of the devices in refs 196 and 197—might lead to a substantial increase in the performance of GNRs fabricated by other techniques (*e.g.*, bottom-up organic synthesis, CVD, electron-beam lithography, *etc.*). However, it is also worth considering other extrinsic factors that can deteriorate the performance of GNR FETs and the means to overcome those factors, which are discussed next.

Extrinsic Barriers to GNR Electronics. i. Contact Resistance. Similar to the fields of CNT and transition metal dichalcogenide (TMD) electronics, a large disparity between theoretical and actual performance of GNR devices can be attributed in part to large contact resistances (R_c) at metal−GNR interfaces and substrate- and dielectric-induced disorder.[257,258] R_c throttles device performance by degrading I_{on}, photoresponsivity, and f_{max}[92,259−261] and is the main parasitic resistance in ultrascaled FETs ($L_{ch} < 20$ nm) in which R_c starts to dominate the total device resistance (due to ballistic transport across the channel, *i.e.*, $R_{ch} \rightarrow 0$).

To date, every GNR device in the literature has been either top- or bottom-contacted (*i.e.*, source/drain metal contacts are deposited on top of GNRs,[89] or GNRs are placed on top of the pre-patterned electrodes).[262] In both of these cases, the GNRs do not form covalent bonds with the contact metal due to their inert basal plane, resulting in poor coupling and a long characteristic "transfer length" (L_T) of ~200 nm (Figure 9a).[263] L_T is the distance over which $1 - e^{-1} \approx 63.21\%$ (where, e is Euler's number ≈ 2.718) of the total current is transferred from the contact metal to the semiconducting channel and characterizes the strength of coupling between the contact and the channel (smaller L_T indicates better coupling).[264] If the contact length (L_c) $\ll L_T$, then poor contacts are obtained in which R_c scales inversely with L_c and is given by $R_c = \frac{\rho_c}{L_c}$, where ρ_c is the contact resistivity.[265] Poor top-contacts and $L_c \ll L_T$ can be problematic under two scenarios. The first scenario occurs when the GNRs are short, and therefore $L_c \ll L_T$, which is common in GNRs that are derived from bottom-up organic synthesis and CVD on Ge(001), as their lengths are only 20−100 nm.[59,89] The second scenario can more generally be problematic for GNRs of any length and occurs when the device footprint must be reduced, for example, to increase FET density in logic circuits. In this case, both L_c and L_{ch} must be reduced to meet geometrical scaling constraints. In both scenarios described above, R_c can become a significant fraction of R_{total} and much larger than the minimum possible intrinsic quantum resistance ($R_{c,int}$) of 12.9 kΩ per GNR.[266,267] Another challenge arises when the fabrication of GNR devices involves transfer of GNRs from a catalyst (*e.g.*, Au or Ge) to a dielectric substrate (*e.g.*, SiO_2), which is typically assisted by a polymer layer and etching of the catalytic substrate. The transfer process introduces adsorbates and contaminants (*e.g.*, polymer and etchant residues) that degrade interfacial quality, add an insulating barrier for charge injection, and/or cause unintentional doping and Fermi-level pinning, each of which further increases R_c.[258,268]

ii. Dielectrics. In addition to contacts, the substrate and/or the gate dielectric can also profoundly impact the performance of GNR FETs. First, the composition and thickness of the gate dielectric impact the electrostatic integrity of the channel and determine the ultimate scalability. The scalability is parametrized by the electrostatic length, λ, which is given as $\sqrt{\frac{\varepsilon_{ch}}{N\varepsilon_{ox}} t_{ch} t_{ox}}$ where ε_{ch} and ε_{ox} are the dielectric constants of the channel and gate oxide, respectively, N is the number of gates, and t_{ch} and t_{ox} are the thicknesses of the channel and gate oxide, respectively.[265] Generally, a channel remains immune to short-channel effects (primarily DIBL and degraded SS) if $L_{ch} \geq 3\lambda$, and therefore, smaller λ is desirable.[269] From the expression, it is evident that a small λ can be achieved *via* reducing t_{ox} and/or increasing ε_{ox}.[125] Second, the substrate and the gate dielectric impact the performance of GNR devices by introducing long-range and/or short-range charge disorder (*e.g.*, roughness and dangling bonds), which degrade μ and cause variation in threshold voltage (V_T).[270,271] GNRs interfaced with common dielectrics, such as SiO_2, Si_3N_4, HfO_2, Al_2O_3, and SiC, show reduced μ (sometimes by several orders of magnitude) compared to theoretically predicted phonon-limited values, which is due to extrinsic scattering from ionized impurities, charge puddles, ripples, surface

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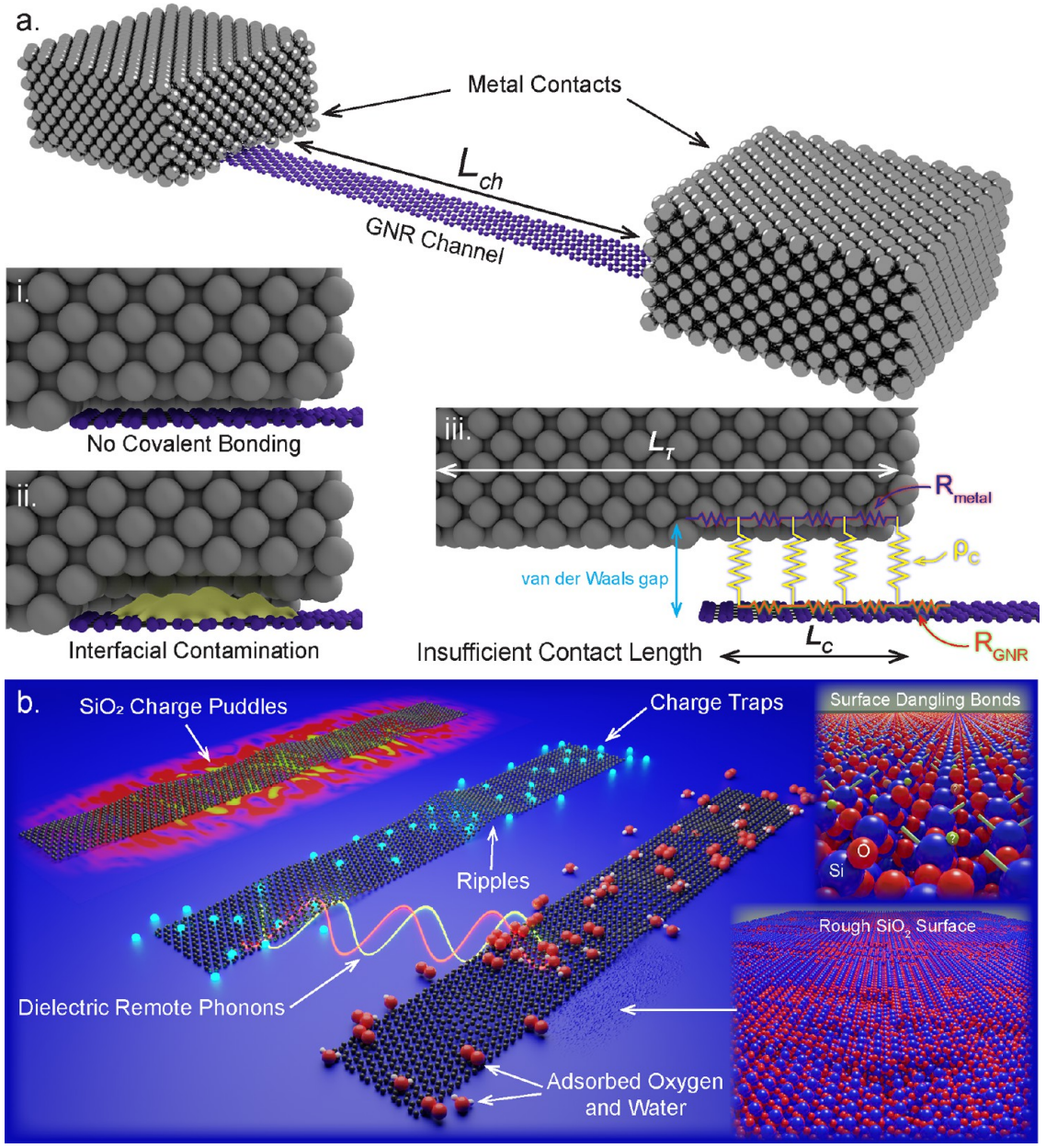

Figure 9. Extrinsic factors affecting the performance of GNR devices. (a) Structure of a typical top-contacted GNR device and the factors causing increased contact resistance: (i) lack of covalent bonding at the interface, (ii) presence of interfacial contamination, and (iii) insufficient contact length ($L_c < L_T$). (b) Combination of factors at the dielectric surface, such as scattering due to phonons, surface roughness, and adsorbed dopants, that cause degraded performance of GNR devices. The sizes of species and features are *not* to scale and are for representation purposes only.

dangling bonds, and dielectric remote phonons (Figure 9b).[74,117,272−278] Furthermore, GNR FETs on oxide substrates measured in ambient laboratory conditions exhibit hysteresis, which likely originates from adsorbed H_2O or O_2 from ambient air and/or traps in the substrate or gate dielectric.[279−281] Therefore, engineering smooth, trap-free interfaces and improved passivation schemes is critical to reduce extrinsic scattering, increase μ, and reduce variation in V_T.

PERSPECTIVES

Overarching Goals in Synthesis. The primary synthesis challenge is to scalably create GNRs with monodisperse widths and smooth edges in tightly packed arrays, with registered placement and alignment on technologically relevant substrates. No existing synthetic method has simultaneously met all these criteria. It is important to emphasize that even an ideal single GNR cannot provide the I_{on} required for most applications. Therefore, GNR FETs need to be fabricated from closely spaced, highly ordered arrays of GNRs—similar to the arrays of CNTs currently being developed for electronics.[227,282−287] Furthermore, precise control over the GNR width and pitch is paramount to achieve uniform FET behavior (*e.g.*, same V_T, I_{off}, and I_{on}), at least for logic and RF applications, while some variability might be acceptable for thin-film/optoelectronic applications.[288,289] The ideal pitch of GNRs is not yet clear; however, modeling of CNT arrays has shown that the ideal pitch of CNTs is 5−10 nm, balancing the need to increase the number of conducting pathways for a

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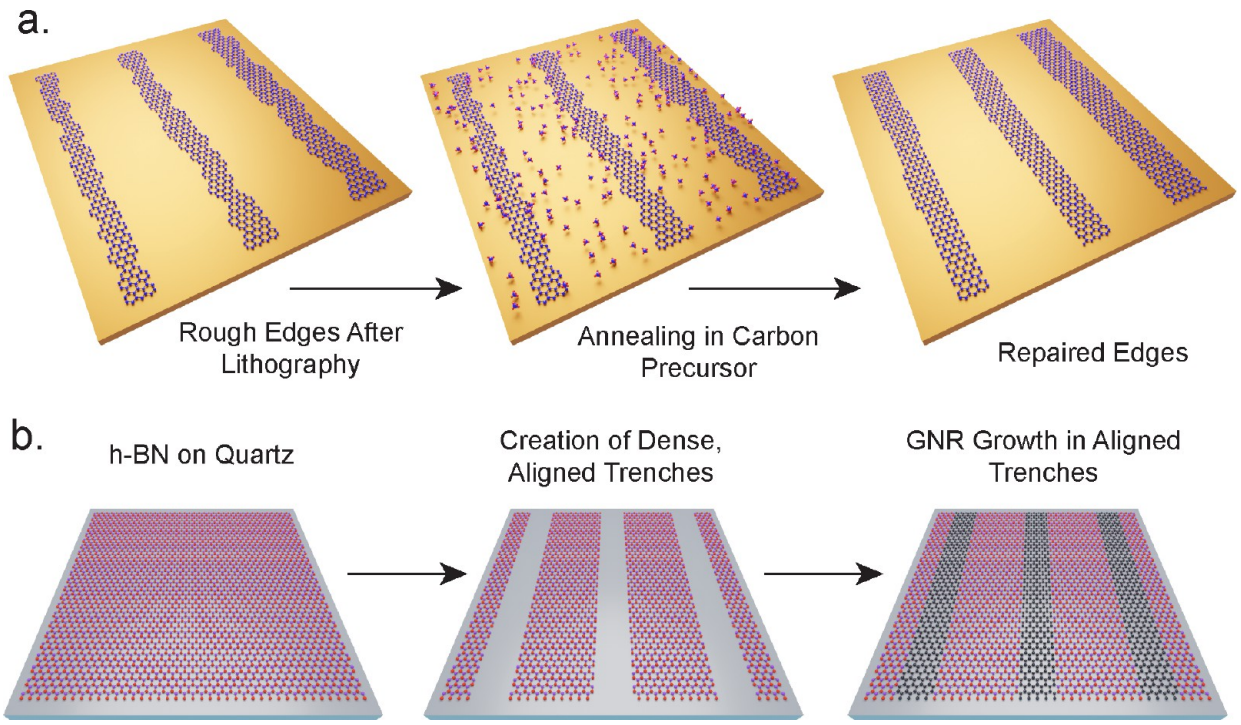

Figure 10. Potential approaches toward overcoming contemporary bottlenecks in lithography and lateral heteroepitaxy for realization of high-performance GNR FETs. (a) Edge-annealing is a potential route to reduce edge roughness in GNRs created by lithography. (b) Lithography can be used to create unidirectional, rationally pitched trenches in h-BN followed by GNR growth to realize FETs with increased I_{on} due to the higher packing density compared to ref 196.

given channel width with the need to limit inter-CNT screening effects that occur when the pitch is small.[290] Although some top-down techniques have been able to realize array GNR FETs,[97,103,291,292] thus far, no GNR array FETs have been realized with high I_{on} and high I_{on}/I_{off}, simultaneously.

Lithography. Unless a scalable lithography technique with much improved resolution is developed, it is not clear if lithography will ever yield sub-10 nm wide GNRs with smooth edges, needed to harness superior electronic properties. There have been a number of promising efforts to pattern sub-10 nm features: notably, directed self-assembly (DSA) of block copolymers, extreme ultraviolet (EUV) lithography, and self-aligned quadruple patterning (SAQP).[293,294] While most experimental and simulation studies agree that edge roughness is detrimental to the performance of GNR FETs,[289,295,296] other works have concluded that a small amount of edge roughness is acceptable and will not significantly degrade the I_{on}/I_{off} or I_{on}.[249] This dichotomy is further evidenced by the demonstration of superior FET performance using GNRs grown heteroepitaxially in h-BN trenches that may possess mixed edge character.[196] Research toward reducing edge roughness, similar to that demonstrated using helium ion lithography[101] and neutral beam etching (instead of reactive-ion etching), could prove useful.[297] Reduction of edge roughness, increased width uniformity, and improved electronic performance might also be achieved, for instance, *via* post-lithography edge-annealing (Figure 10a),[298,299] controlled gas-phase/plasma etching,[107,108] and passivation schemes such as hydrogenation.[300,301]

In-Plane Heteroepitaxy with Hexagonal Boron Nitride (h-BN). As discussed previously, sub-10 nm GNRs grown in h-BN trenches exhibit among the best combination of G_{on} and I_{on}/I_{off} observed in the literature.[196,197] Therefore, the in-plane heteroepitaxy of GNRs from the edges of h-BN, of GNRs in h-BN nanotrenches, and of h-BN from the edges of GNRs could all be promising routes toward high-performance GNR electronics. Moving forward, the field needs to move beyond single GNRs embedded in h-BN toward creating tightly pitched, aligned arrays of embedded GNRs (Figure 10b), which will be paramount for increasing I_{on} for high-performance applications. It may be possible to exploit directional, metal nanoparticle-assisted etching to create such arrays. However, particularly significant challenges are that (i) the nanoparticles may etch stochastically along several directions, and (ii) the nanoparticles themselves are polydisperse.[302] Significantly improved control over trench-orientation, edge topology (armchair versus zigzag), placement, and width is needed. As a first step toward this end, arrays of GNRs have been created by the directional metal-assisted etching of graphene[303]—although these arrays have not yet offered the control over width, pitch, and placement required. An alternative may be to use lithography to define trenches, coupled with recent advances in the CVD of graphene from the edges of h-BN and *vice versa*.[304,305] Increased research activity focusing on lateral heteroepitaxy within the 2D materials community[306] may yield additional strategies for synthesizing GNR–h-BN lateral heterojunctions in the future. Theoretical modeling of electronic properties will also be needed to reconcile the differences in band gaps observed between GNRs embedded in h-BN and GNRs synthesized by polymerization and graphite/CNT unzipping.[196,307–309] This modeling will be critical for developing a comprehensive understanding of the effects of edge termination, lattice strain,[310–312] and edge passivation[300,313] on h-BN/GNR FET

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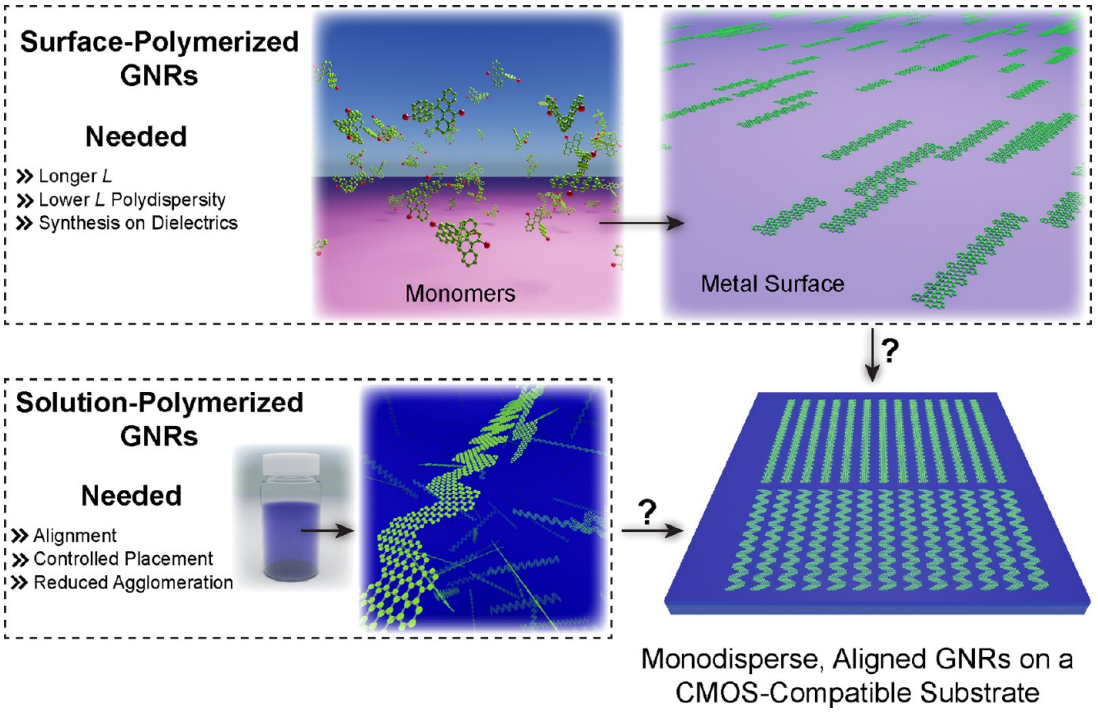

Figure 11. Primary challenges blocking integration of (a) surface-polymerized GNRs and (b) solution-polymerized GNRs into technology.

behavior[302,314−316] in addition to discerning the role of the underlying substrate.

Bottom-Up Organic Synthesis. The fields of on-surface and solution-mediated organic synthesis have made impressive advances toward producing complex and atomically precise GNRs, yet the FETs from these devices have significant room for improvement. Whether extrinsic factors or possible intrinsic edge roughness in these GNRs is the predominant cause of suboptimal performance is a question that will require more comprehensive studies.[187] If edge roughness is present, its reduction will necessitate a careful evaluation of precursor selection and control over reaction chemistry.

Next, even though the synthesis and self-assembly of densely aligned GNRs have been reported on Au(788) and Au(111), respectively,[148,189] better control over pitch and placement is still needed (Figure 11). Improved control over pitch is especially important because if the pitch is too high, crosstalk and screening effects degrade gate control of the channel, leading to poor I_{on}, I_{on}/I_{off}, SS, DIBL, and f_{max}.[190,290,317] When top-contacts are used, longer surface-polymerized GNRs are required to improve $2R_c$ by ensuring $L_c \gg L_T$. Direct synthesis on dielectrics (as opposed to metallic surfaces) would also be needed for electronics applications. Toward this end, ref 318 has recently demonstrated the catalyst-independent synthesis of polyaromatic azaullazine chains *via* polymerization of polycyclic aromatic azomethine ylides on h-BN, and ref 319 has recently shown the synthesis of armchair GNRs on insulating TiO_2 surfaces, both of which are promising breakthroughs motivating further research into engineering monomers that polymerize on nonmetallic surfaces. The use of polymerized GNRs in thin-film transistors, in which the channels are longer than the individual GNRs, necessitates synthesis of longer GNRs and networks of GNRs interlinked *via* covalent bonds to achieve a satisfactory μ.[320,321] Here, it is particularly attractive to use an on-surface polymerized graphene nanomesh as a channel, which is easier to transfer from Au(111) to a target substrate than arrays of isolated GNRs and can exhibit electronic properties (G_{on} and I_{on}/I_{off}) comparable to those of individual GNRs.[322−324]

Meanwhile, advances in shear-assisted wafer-scale alignment of CNTs from bulk solution or liquid/liquid interfaces,[325−327] Langmuir−Blodgett assembly of dense and aligned CNT films,[328] dielectrophoretic self-assembly of graphene,[329] and electric-field-induced alignment of GNRs[330] could be explored for the alignment and self-assembly of solution-polymerized GNRs, although control over pitch might still be challenging. A significant improvement in alignment and density, and consequently the charge transport through such random networks of GNRs, might be achieved by appropriate non-covalent surface functionalization or substrate modification, as seen in drop-cast CNT thin-film FETs fabricated on substrates grafted with self-assembled monolayers.[331−333] Clearly, more research into tailoring surface chemistry to achieve high density, uniformity, and alignment of deposited GNR thin films is needed.[334] Furthermore, as recently demonstrated for CNTs, it may also be possible to precisely deposit GNRs from solution with controlled placement *via* directed self-assembly strategies with DNA nanotrenches.[284,285] It is also important to note that improved strategies are needed to inhibit side-reactions that generate a mixture of GNR structures in some solution-phase syntheses (*e.g.*, preventing isomerization during Diels−Alder polymerization reactions), and eventually, the effect of extrinsic impurities on the charge transport properties of GNR thin films will need to be clarified.[335−338] Lastly, standardized protocols for the unambiguous characterization of the structural (*e.g.*, length and defects) and electronic (*e.g.*, band gap) properties of polymerized GNRs, on surfaces and in solution, are also currently underdeveloped but needed.[174,339,340]

CVD on Ge. Regarding CVD synthesis on Ge or similar surfaces that might promote anisotropic growth, challenges include (1) obtaining more accurate control over width with

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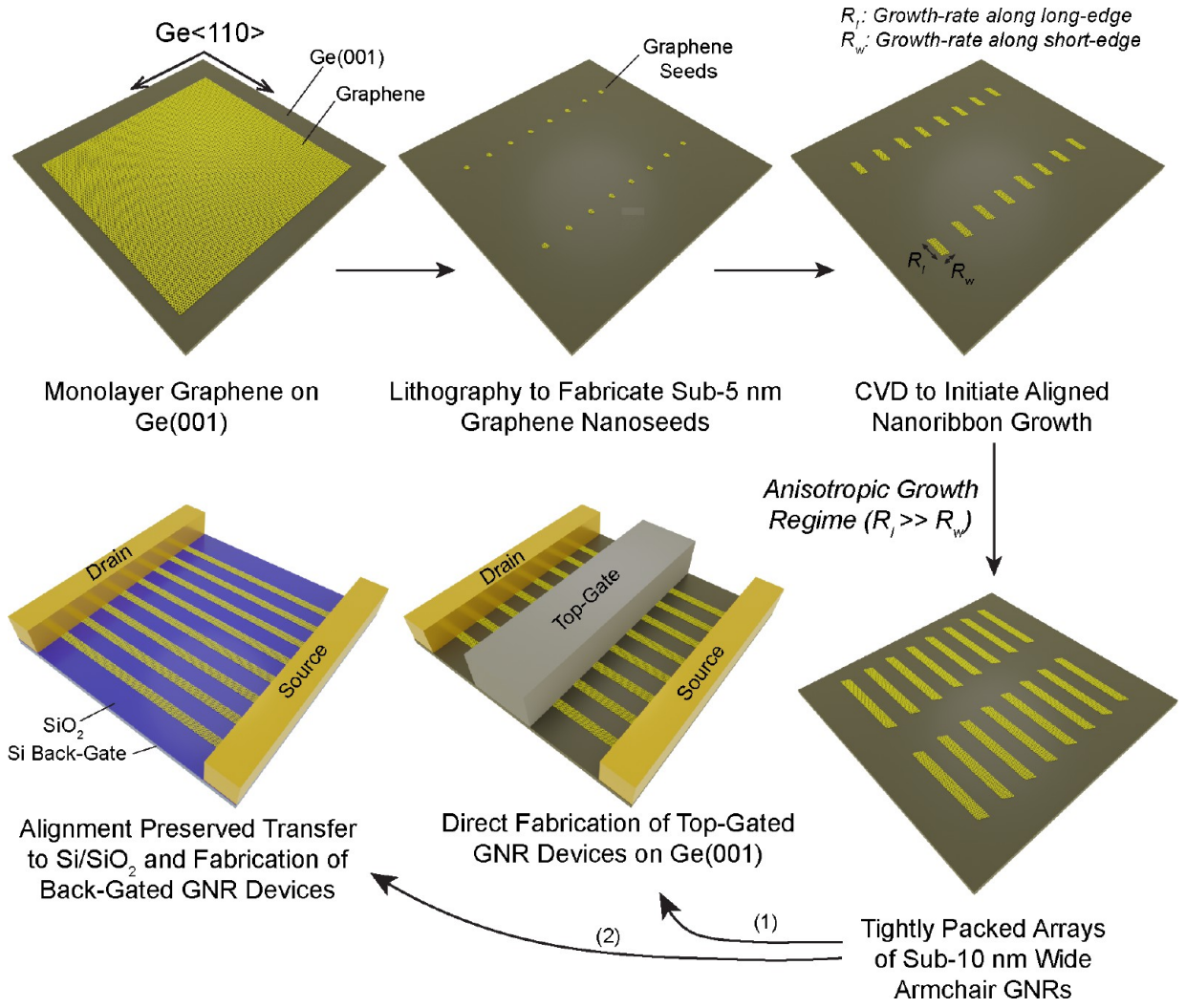

Figure 12. Initiating synthesis of tightly packed arrays of sub-10 nm armchair GNRs *via* CVD by deterministically placing sub-5 nm graphene seeds, followed by direct fabrication of top-gated devices on Ge(001) or transfer to dielectric surfaces for fabrication of back-gated devices.

less GNR-to-GNR variation; (2) realizing densely packed arrays of aligned GNRs; (3) improving the transport properties of these GNRs; (4) reducing the CVD thermal budget; and (5) transfer-free integration on CMOS-compatible platforms. With regards to challenges 1 and 2, significant progress has been made toward fabricating aligned GNR arrays on Ge(001) with reduced polydispersity *via* seeding and conducting growth on vicinal Ge(001) surfaces.[73,341] However, the seed-initiated GNRs demonstrated on Ge(001) have been super-10 nm wide, can rotate as the GNR width decreases, and still suffer from GNR-to-GNR variation in width due to challenges in achieving small and uniform seeds *via* lithography.[342] More work is needed to reduce pitch, decrease seed size, and improve seed uniformity in order to realize dense unidirectional arrays of more monodisperse sub-5 nm GNRs (Figure 12). One approach to realizing tightly pitched sub-5 nm seeds could be to exploit directed self-assembly using block copolymers in combination with infiltration synthesis.[294,343−345] Regarding challenge 3, devices realizing high G_{on} approaching the quantum conductance limit of 77 μS ($2e^2/h$) still need to be demonstrated. The GNRs synthesized on Ge have long segments of smooth armchair edges, but more work is needed to elucidate the potential effect of the minor edge roughness that may exist on charge transport properties. For challenge 4, methodologies to reduce the catalytic barrier for the decomposition of hydrocarbon precursors on the Ge(001) surface need to be explored. Here, advances in low-temperature synthesis of graphene could provide useful guidance. Possible solutions include exploration of liquid precursors, such as benzene and toluene, that have been utilized to synthesize graphene at temperatures as low as 300 °C[346] and the use of energy-assisted CVD techniques [*e.g.*, microwave plasma (MPCVD), photothermal (PTCVD), plasma-enhanced (PECVD), and inductively coupled plasma (ICPCVD), *etc.*] that have been utilized to synthesize graphene at temperatures below 500 °C.[347−350] Regarding challenge 5, more work is needed to fabricate and measure GNR devices directly on Ge or Ge-on-Si(001). Specifically, it is critical to decouple GNRs from the Ge surface and minimize the vacancy-induced doping of the Ge substrate at the high temperatures used in CVD.[226] The latter could enable the direct fabrication of top-gated GNR devices on Ge(001). The formation of stable, uniform films of Ge oxide underneath GNRs *via* thermal oxidation or electrochemical intercalation could be explored.[351] Alternatively, for GNRs synthesized on Ge-on-Si(001), alignment-preserved transfer to Si(001) *via* chemical vapor etching of the Ge epilayer or *via* wafer-bonding could be investigated (Figure 12).[352] The latter could be feasible considering the recent

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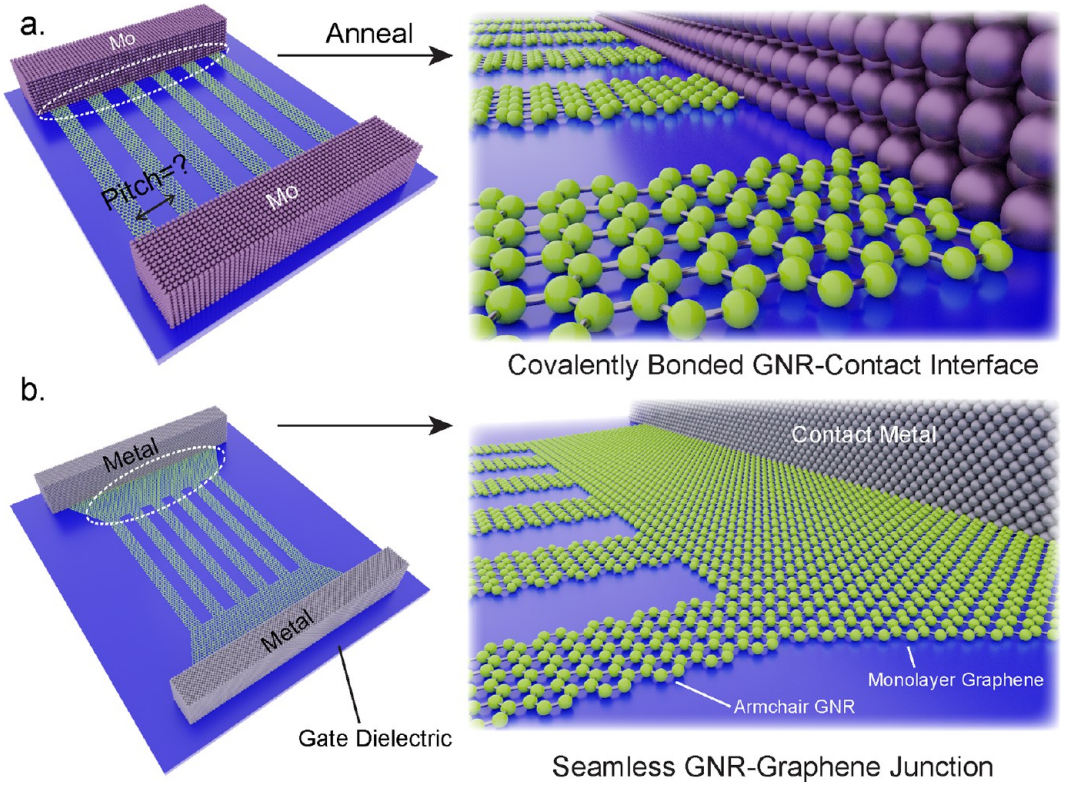

Figure 13. Edge-bonded schemes to achieve contacts with low R_c in GNR devices. (a) Forming a covalently bonded GNR−contact interface by deposition of Mo electrodes followed by annealing, which forms interfacial carbides. (b) Forming seamless junctions between arrays of semiconducting armchair GNRs and semimetallic monolayer graphene.

demonstration of a stacked Ge-based gate-all-around FET (GAAFET) PMOS layer atop Si-based FinFET NMOS *via* a wafer-bonding process.[353]

Materials and Device Integration. *Contact Resistance.* Major approaches to reduce R_c include (1) developing a contamination- and residue-free method to transfer GNRs to technologically useful dielectric substrates, (2) reducing the metal−GNR contact resistivity (ρ_c), and (3) reducing Schottky barriers by work-function engineering of the contact metal or doping of the contact area.

With regards to approach 1, it is crucial to develop a scalable, clean, and automated transfer technique that preserves the intrinsic properties of GNRs synthesized on non-dielectric surfaces (*e.g.*, organic synthesis, CVD, *etc.*). A possible reason behind the superior charge transport properties of GNRs synthesized on SiC nanofacets, when compared to other techniques such as on-surface polymerization and CVD, could be the absence of a transfer step in these techniques, ensuring a relatively cleaner GNR interface. Several promising techniques for support-free transfer of graphene have been developed but have not yet been explored for transfer of GNRs.[354,355] Meanwhile, other approaches—such as exposure to low-power plasma, UV/ozone treatment, use of sacrificial layers, and postannealing—have been beneficial in reducing resist residues and adsorbed contaminants on graphene, reducing R_c by up to 5000 times in graphene devices.[356−358] R_c in graphene devices has also been shown to significantly diminish by implementing "metal-on-bottom" (*i.e.*, graphene is placed on top of predeposited metal contacts) or "double contact" (*i.e.*, graphene is sandwiched between metal contacts) architectures, which lead to much cleaner interfaces and enhanced contact area, respectively, compared to typical "metal-on-top" contact architectures. These concepts might also lead to reduction of R_c in GNR devices.[359,360] GNR transfer and device fabrication could also be simplified *via* adhesion engineering (*i.e.*, engineering delamination of GNRs from the catalyst) and leveraging recent breakthroughs in robot-assisted assembly of van der Waals heterostructures—reducing the possibility for inadvertent extrinsic contamination.[361] In general, an improved understanding of the effect of residue (including its thickness and composition) on R_c is needed.[362]

Regarding approach 2, low R_c can potentially be realized by degenerate doping of the contact area. Doping of the contact area using layers of dopant species has been demonstrated to yield low-R_c metal−graphene contacts by reducing the tunnel barrier width and increasing the density of states;[363] however, so far, such doping has been difficult to control or has long-term stability issues and can consequently lead to variation in V_T and high I_{off}.[364] Therefore, better doping species and methods that yield improved control and stability are needed. For example, GNRs synthesized by polymerization can be substitutionally doped by utilizing tailored precursors.[365,366] For less aggressively scaled applications (*e.g.*, low-power RF and thin-film transistors), longer contact lengths could help reduce R_c. This is because for $L_c \gg L_T$, R_c saturates invariant of L_c, and this could explain the superior I_{on} in FETs with relatively long GNRs (and therefore long L_c) that are fabricated from top-down sonochemical unzipping of graphite and in-plane heteroepitaxy in h-BN trenches.

However, for ultrascaled GNR FETs (L_{ch} < 20 nm), where ultrashort L_c is required to maximize the FET density, large R_c is a major roadblock. In this case, edge contacts, in which GNRs are covalently bonded to the contact material, or a

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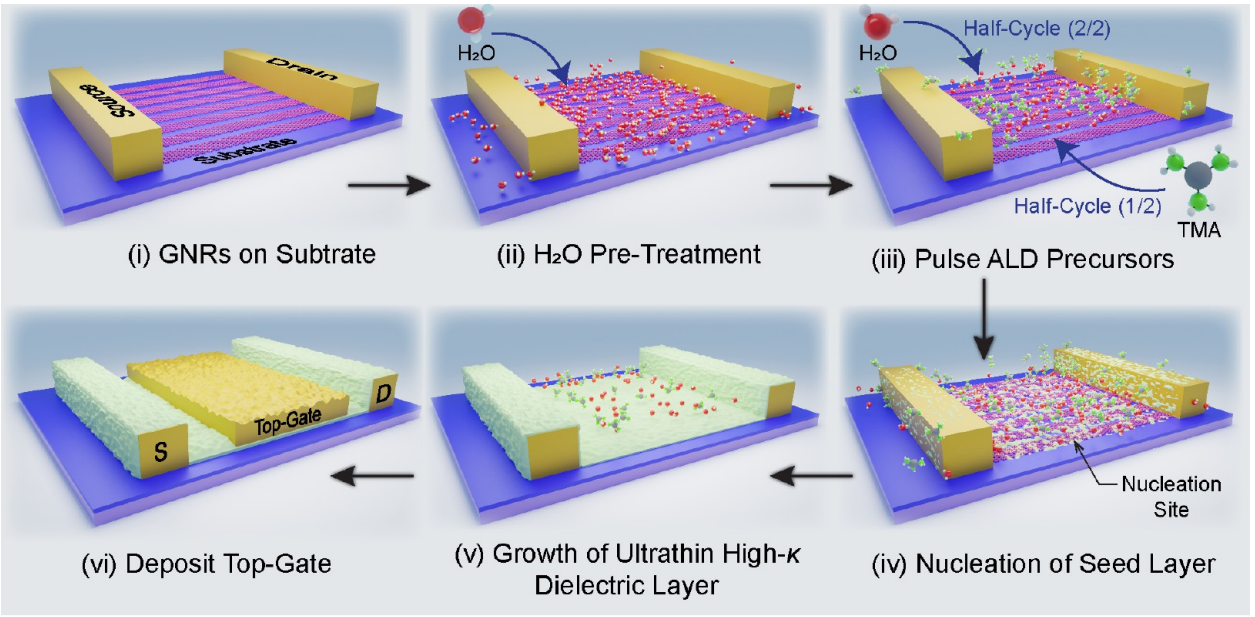

Figure 14. Integration of high-κ dielectric top gates on GNR FETs *via* atomic layer deposition (ALD), adapted from refs 404, 408, 409, 416, and 428. An analogous method has been experimentally demonstrated for ALD of high-κ dielectrics on graphene and CNTs. (i, ii) Pretreatment with gaseous H_2O to promote conformal nucleation. (iii, iv) Cycle ALD precursors (trimethylaluminum (TMA) and H_2O) to nucleate Al_2O_3. (v) Grow Al_2O_3 *via* ALD. (vi) Deposit top-gate metal.

combination of top and edge contacts must be explored (Figure 13a). Edge contacts can enable aggressive contact scaling since carrier injection is independent of L_c, enabling lower R_c than contemporary top-contact schemes by an order of magnitude, as predicted theoretically[367,368] and demonstrated experimentally for graphene[369−372] and CNT devices.[373] For example, Mo[373] and Co−Mo[227] yield interfacial Mo−C carbides upon annealing on graphene and CNTs at 150−800 °C, facilitating formation of edge contacts.[371] Mo-based edge contacts have resulted in low R_c with CNTs, even down to L_c < 10 nm,[373] and therefore could be a promising route to reduce R_c and enable aggressive contact scaling in GNR devices (Figure 13a). Ni/Al edge contacts to graphene have also resulted in low R_c, which is particularly appealing because these materials are CMOS-compatible.[372] MoO_{3-x}, another high-work-function contact material that exhibits far superior hole-injection to transition metal dichalcogenides than Pd, and that has been recently demonstrated to yield low R_c edge contacts to graphene, could also be exploited for GNR devices.[371,374] However, engineering edge contacts for GNR devices has not yet been reported, necessitating further research in this direction. Controlled plasma treatment can also be utilized to create dangling bonds at the short edges of GNRs, which are required to form covalently bonded edge contacts.[375] Another option is to create seamlessly bonded junctions between semiconducting armchair GNRs and metallic zigzag GNRs or graphene[376−379] (Figure 13b), similar to phase-engineered contacts in MoS_2 or intramolecular CNT−GNR junctions.[267,380,381] In recent studies, devices consisting of polymerized GNRs contacted with monolayer graphene were demonstrated; however, the GNR−graphene junctions were not covalently bonded but were instead in van der Waals (vdW) contact.[92,172,262] However, even such contacts might provide the possibility of achieving sub-60 mV dec^{-1} SS similar to the recent demonstration of CNT devices consisting of graphene as a Dirac source to achieve an SS of 35 mV dec^{-1},[382] and some computational studies have predicted an astonishingly low L_T = 10 nm for such GNR−graphene van der Waals contacts.[383]

Lastly (approach 3), the choice of metal for the source/drain electrodes, method of deposition, and deposition conditions ostensibly impact R_c due to the formation of interfacial traps, Schottky barriers (SB), and modification of the graphene sheet resistance under the contacts (due to charge-transfer doping and Fermi-level pinning).[364,384−386] For GNR FETs measured on SiO_2, *p*-type conduction is observed, presumably due to doping during transfer, inadvertent edge-functionalization during solution processing, and/or exposure to ambient air.[172,387] Therefore, high-work-function metal contacts are used to make good *p*-type contacts with low SBs. It is however also believed that the apparent *p*-type conduction might be due to adsorbed H_2O adlayers on the SiO_2 that suppress *n*-type behavior.[388] A better understanding of the underlying mechanisms, improved encapsulation schemes,[389] and/or surface treatment techniques[390] is needed to overcome the above issues in order to select the best contact metal.[391] Next, the carrier transmission probability from metal to graphene, which depends on coupling between metal and graphene, greatly affects the R_c.[268] Metals such as Ni, Co, Pd, and Ti that chemisorb on graphene form much lower R_c contacts, as opposed to metals such as Au and Pt that physisorb.[391,392] Pd, in particular, has been the preferred choice for contact metal in GNR devices due to its deep work function, which leads to low SBs with GNRs that are presumably *p*-doped, as discussed above.[72,90,196,393,394] Often, a thin layer of Cr, Ti, *etc.* is also used to enhance adhesion between Pd and the GNR, although it is not clear if these interfacial layers play a role in modifying R_c. Ohmic contacts may even be possible by either utilizing contact materials that form a negative SB to GNRs or by intercalating oxides, such as Ta_2O_5, TiO_2, or MgO, that can unpin the metal Fermi-level at the contact interface.[395,396] Alternate metallization schemes (*e.g.*, atomic layer deposition)

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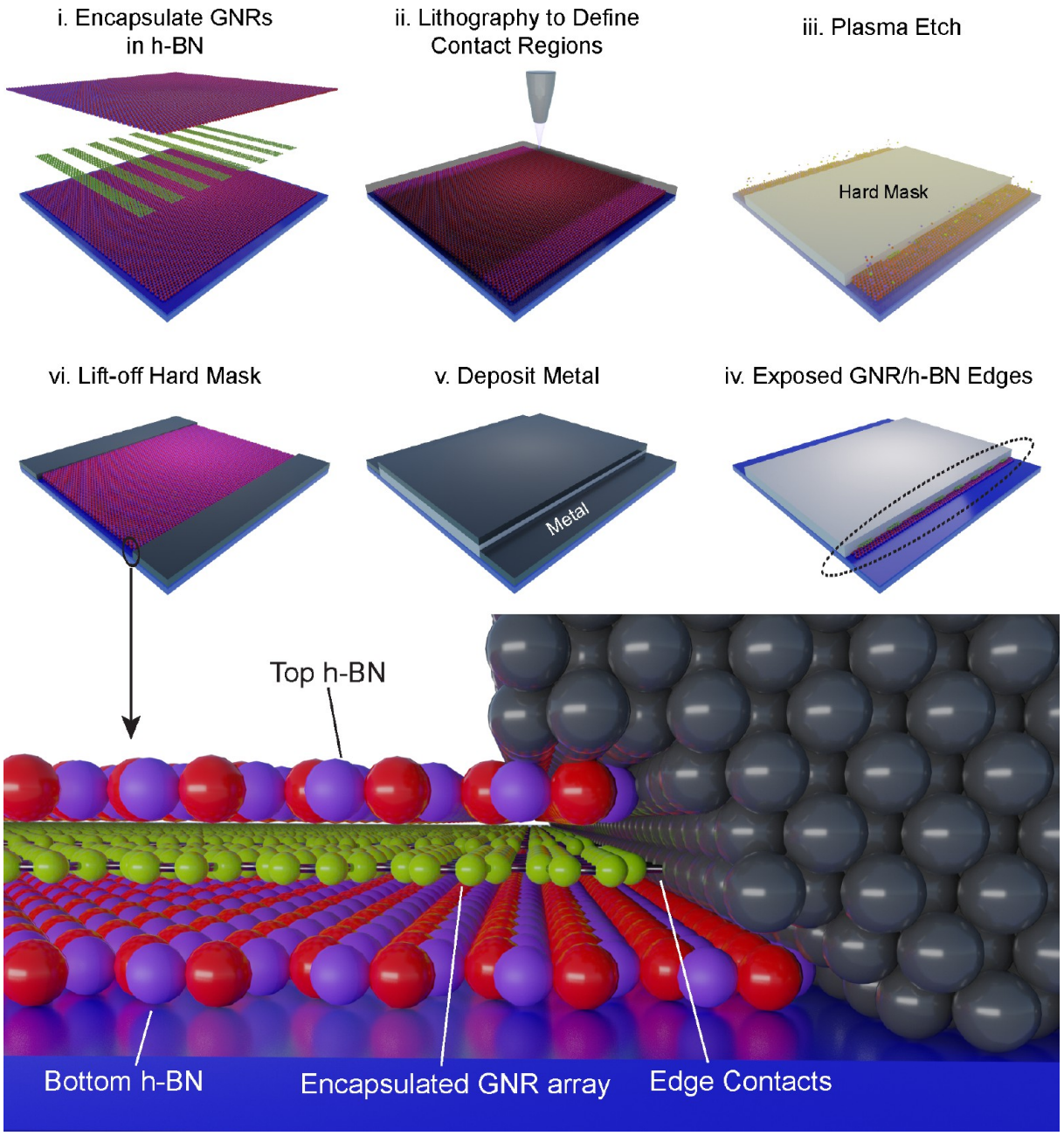

Figure 15. Possible approach toward fabricating GNR arrays encapsulated in h-BN, similar to the one demonstrated in ref 369 for monolayer graphene. This technique also allows for 1D edge contacts to be formed.

instead of evaporation/sputtering can also be explored to improve the morphology of the deposited metal in order to enhance the coupling between the metal and the GNR.[397] High-quality contacts may also be fabricated by utilizing thermal scanning probe lithography, which has a comparable throughput and resolution as electron-beam lithography.[398] Optimization of source/drain geometry in GNR FETs is also a promising route to reduce R_c.[399]

Substrate and Dielectric. Another challenge in GNR electronics is the optimal selection of substrate and/or gate dielectric. So far, nearly all GNR FETs in the literature utilize a SiO_2 global back gate due to relative ease of fabrication; top-gated GNR FETs remain largely unexplored. However, top gates are paramount in order to switch individual FETs, independently in an integrated circuit. Although some studies have demonstrated GNR devices with core−shell nanowires as top gates and achieved large transconductance, it is not clear if control over the position/orientation of these nanowires can be realized on prefabricated GNR arrays.[124] Generally, the fabrication of top gates requires conformal deposition of ultrathin dielectrics, which is typically accomplished by atomic layer deposition (ALD). However, uniform ALD on pristine or uncontaminated surfaces of graphene/CNTs/GNRs/2D materials is challenged by their inert basal planes and the absence of dangling bonds and defects.[287,400,401] Surface treatments such as UV/ozone, electron-beam irradiation, and plasma exposure have been used to seed the growth of dielectrics on graphene and CNTs. These treatments introduce defects in the sp^2 basal plane that enable chemical adsorption/bonding of the dielectric precursors.[402−405] The ensuing distorted lattice of

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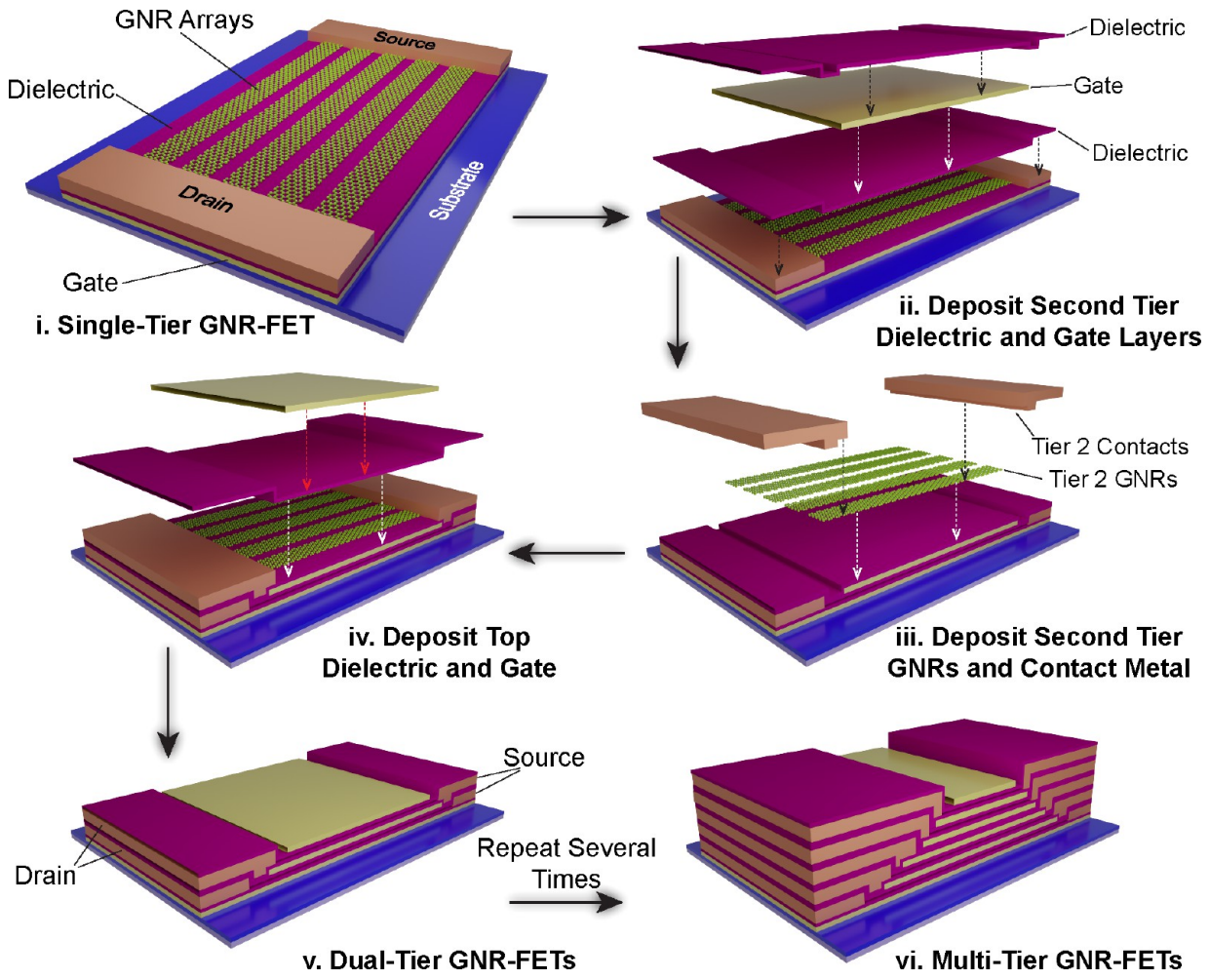

Figure 16. Multitier GNR FETs may increase I_{on} within a given footprint without needing ultrashort channel length. Concept adapted from ref 445 which demonstrates a similar idea for MoS_2 FETs.

the CNT or GNR is known to degrade the transport properties of these transistor channels. Therefore, such treatments are likely to be unacceptable for GNRs since the integrity of the basal plane and edges is paramount to retaining intrinsic charge transport properties. A possible solution here might be using H_2 plasma to seed the deposition of dielectrics, wherein the H-functionalization of the graphitic lattice is reversible upon annealing.[406] However, full reversibility of the damage by the annealing is unlikely in large-scale integration. Consequently, clever nucleation engineering solutions based on physical adsorption of precursors are necessary. Some reports have indicated that *in situ* pretreatments or noncovalent surface functionalization (*e.g.*, introducing pulses of H_2O, O_3, NO_2/trimethylaluminum (TMA)) prior to ALD can significantly improve the homogeneity and quality of the deposited films on graphene and CNTs, leading to superior device performance without affecting the quality of the channel; however, it is not yet clear if such approaches would work for GNRs (Figure 14).[407−411] The use of organic (*e.g.*, perylene tetracarboxylic dianhydride (PTCDA), hydrogen silsesquioxane (HSQ), *etc.*), polymer (*e.g.*, polyvinyl alcohol (PVA)), ultrathin metal seed (*e.g.*, Ti), or metal-oxide (*e.g.*, yttrium oxide (Y_2O_3)) interlayers can also improve the quality of the dielectric films,[412−414] and a recent report has achieved an equivalent oxide thickness (EOT) of 1 nm using PTCDA to seed ultrathin hafnium oxide (HfO_2) on graphene and MoS_2.[415] On CNTs and graphene, deposition of a metal (which coats the inert sp^2 lattice more uniformly than its corresponding metal oxide) followed by oxidation has been used to create a seed layer for dielectric deposition *via* ALD (*e.g.*, Ti followed by oxidation to TiO_2 and then Al_2O_3 deposition).[416] Alternatively, the oxidized metal layer can also be directly used as the dielectric layer. ALD of dielectrics can also be circumvented altogether by transferring gate stacks and by utilizing pre-embedded gates.[417,418]

As for materials, the incorporation of high-k dielectrics such as Al_2O_3 (ε = 9), Y_2O_3 (ε = 15), HfO_2 (ε = 16.5), and lead zirconate titanate (PZT) (ε = 350) is paramount for realizing superior electrostatic modulation of the channel at scaled gate lengths (to minimize λ and suppress band-to-band tunneling and for enhancing dielectric screening from charged impurities to obtain higher μ).[225,419,420] Y_2O_3 in particular is a promising dielectric material for GNR FETs because it is relatively simple to deposit on sp^2 carbon nanomaterials (deposited as Y and subsequently oxidized) and has demonstrated high capacitance while preserving high μ in graphene.[421,422] More research is also needed to identify and incorporate alternative dielectrics, such as AlN (ε = 9) and ZrO_2 (ε = 23), and interfacial passivation layers, such as BeO, that exhibit reduced phonon scattering when graphene is placed on these materials compared to SiO_2 or HfO_2.[423−426] The addition of a ferroelectric material such as hafnium-zirconium oxide, which enables negative capacitance, to the gate-stack may increase

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channel−gate coupling to further reduce the SS below the Boltzmann limit of 60 mV dec^{-1} and enhance I_{on}.[427]

Placing GNRs on and encapsulating GNRs in h-BN is another appealing approach to improve device performance due to the passivated, clean, flat, and highly crystalline surface of h-BN with high optical phonon energy, which leads to higher μ and spin-diffusion lifetimes in graphene[429−431] and GNRs.[432] For instance, room-temperature μ of carriers in graphene placed on h-BN can reach ~10^5 cm^2 V^{-1} s^{-1}, which is close to the theoretical maximum limited by phonon scattering in graphene, whereas, on SiO_2, μ is limited to ~10^4 cm^2 V^{-1} s^{-1}.[433,434] Encapsulation of graphene with h-BN in combination with edge-bonded contacts has also dramatically reduced R_c.[435] Additionally, h-BN can be used as a "contact transfer" layer, wherein the contact metal can be embedded in prepatterned h-BN and directly transferred onto the GNR channel, making via-contacts,[436] reducing interfacial contamination and roughness and consequently R_c.[437] The high in-plane thermal conductivity of h-BN might be particularly useful for rapid heat transfer from GNRs to metal contacts. h-BN might also be useful for FETs integrated on flexible substrates because of its mechanical resilience.[438] Therefore, GNR FETs encapsulated in h-BN could reap several benefits such as high μ, low R_c, superior thermal management, and passivation (Figure 15). Substantial improvements in the scalable production of high-quality h-BN on metallic[439] and dielectric substrates[440] have recently been reported, and GNR-transfer and GNR-transport characterization on h-BN are actively underway.[441] Additionally, an h-BN-assisted "contact and peel" technique of transferring uniform graphene layers from Ge(110) to arbitrary substrates has been reported,[442] which can be explored for the polymer-free transfer of CVD-synthesized GNRs from Ge(001) with h-BN encapsulation. A challenge with h-BN in FETs is its relatively low dielectric constant, which can lead to leakage currents and prevent the equivalent oxide thickness (EOT) scaling (~1 nm) required for ultrascaled MOSFETs.[443] Consequently, more research is required to identify and integrate other high-k dielectrics that deliver similar benefits as h-BN.[444]

Further Device Architectures and Concepts. Beyond traditional applications, there are several approaches to harness the potential of GNRs. One option is to stack tiers of GNR devices vertically, increasing integration density (also known as monolithic 3D integration or M3D) and performance (*e.g.*, higher drive current per footprint) due to effective width scaling (Figure 16).[445] GNRs are front-runners for future M3D-architectures due to their high thermal conductivity, enabling efficient heat dissipation, and their atomically thin bodies, enabling smaller tier thickness and ~150% higher packing efficiency than M3D-integrated bulk semiconductors.[446,447] M3D-architectures promise to achieve a high I_{on} comparable to ultrascaled FETs but at relatively longer channel lengths. However, a primary challenge is producing GNRs at temperatures of <500 °C that are compatible with back-end-of-line processing, because in M3D-integration, temperatures of underlying tiers cannot exceed 500 °C. Low-temperature GNR production has been elusive in many approaches (*e.g.*, CVD, templated synthesis, lateral heteroepitaxy, *etc.*). Direct growth of doped multilayered GNRs at 300 °C has been reported by pressure-assisted solid-phase diffusion, although more work is needed to control layer number, width, and edge roughness and to evaluate the crystalline quality and charge transport properties.[448,449] Parallelly, methods for transferring and stacking of aligned GNRs (similar to stacked nanowires) such as contact-printing need to be explored.[450,451]

Architectures beyond the conventional Schottky barrier GNR FET design can also be exploited.[121] For example, heavily doped source/drain contacts can be used like in Si MOSFETs, which could potentially eliminate the Schottky barrier and increase G_{on} and g_m. Such architectures are expected to improve f_T and reduce intrinsic delay by 30% and 17%, respectively, in RF devices.[452] Suppression of short-channel effects is also expected *via* the use of dual material gates,[452] side gates,[453] asymmetric gates,[454] halo-doping,[455] and junctionless channels.[65] GNR devices based on band-to-band tunneling (*e.g.*, tunnel FETs (TFETs)) and spintronics (*e.g.*, spin FETs, spin LEDs, *etc.*) should also be investigated. TFETs can achieve SS smaller than the Boltzmann limit of 60 mV dec^{-1}, high I_{on}/I_{off}, and superior drain saturation, making them promising for low-power logic and RF applications. GNRs are particularly attractive in TFETs due to their direct band gap, symmetric band structure, and light m_{eff}, which facilitate band-to-band and intraband tunneling[456] and lead to higher I_{on} and lower SS than Si TFETs. In fact, GNR TFETs are predicted to have the lowest energy-delay-product of all low-power switching technologies.[456−458] Experimentally, TFETs based on 2D materials such as MoS_2 and lithographically patterned GNRs have already been demonstrated, validating the feasibility of this technology.[125,459] Future research should aim to incorporate GNRs with atomically smooth edges and controllably doped source/drain regions for improved TFET characteristics such as high I_{on} and I_{on}/I_{off}.

Spintronics may usher in a distinct era of devices for memory, spin-configurable logic, and quantum computing. However, realization of spintronic devices requires long spin lifetimes (~100 μs), long spin diffusion lengths, high μ, and low spin−orbit coupling. Recent breakthroughs in the synthesis of GNRs with precise edge structures, chemical functionalization, and topology present a breadth of interesting opportunities for the exploration of exotic spintronic and quantum phenomena in GNR devices.[43,48,156,460−463] For instance, recent significant advances in the synthesis of zigzag GNRs,[147] GNRs functionalized with spin-bearing groups,[48,156,462,464,465] and GNRs with engineered magnetic topological defects have demonstrated the promise of spin qubits in GNRs. Stable magnetic ordering is also theoretically predicted in doped-armchair GNRs, and quantum logic gates harnessing plasmons in GNRs have been proposed.[80,466] Moreover, theoretical calculations show that h-BN can induce spin-splitting in zigzag GNRs, rendering them half-metallic.[467] Experimentally, however, validation of such theoretical models is lacking, and further investigation of edge magnetism *via* characterization tools such as spin-polarized STM or electron spin resonance (EPR) spectroscopy is needed.[141] Furthermore, the influences of extrinsic factors (*e.g.*, substrate, contaminants, defects, *etc.*), edge functionalization, and doping on spin density and decoherence need to be further studied, and challenges such as inefficient spin-injection/spin-dephasing induced by contacts need to be overcome.[468]

As mentioned previously, integrating GNRs in lower-level (M0, M1) interconnect layers can enable interconnect scaling to sub-10 nm wire thicknesses beyond what would be nominally possible with existing materials such as Cu or Co that are plagued by electromigration.[469] Alternatively, because graphene acts as an excellent barrier to Cu diffusion, replacing barrier (or liner) layers (that are several nanometers thick)

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with atomically thin graphene can enhance the percent Cu fill and reduce the interconnect resistance.[470−472] The primary challenge therefore lies in developing BEOL-compatible integration solutions that would yield GNRs at deterministic locations. $FeCl_3$-doped multilayered GNRs have been shown to exhibit impressive current carrying capacity; however, the long-term operational stability (over several months) and impact of such a doping on surface- and line-edge roughness and functionalization of multilayered GNRs needs to be studied in more detail.[448,473] Although some ideas have been conceptualized,[24,474] it is also not yet clear how such doped multilayered GNRs might be incorporated vertically in high-aspect-ratio vias without a wet-transfer process, with high yield, and control over GNR chirality. Furthermore, formation of low-resistance end-contacts between GNR-interconnects and FET contact plugs remains to be explored, as it would be paramount to ensure that the overall interconnect delay remains low.[475]

Computational/Theoretical Modeling. Modeling of the physics, scaling, and performance of GNR FETs will also enable future breakthroughs.[476] Some computational studies have predicted that GNR FETs will be plagued by source-to-drain tunneling in the L_{ch} < 10 nm regime.[477,478] However, similar computational predictions for CNTs were also made initially but were later invalidated experimentally. This disagreement has been attributed to a lack of understanding of carrier transport in/at/through metal−CNT contacts.[479] Indeed, more work is needed to understand the role of the Schottky barrier, metal-induced gap states, and charge transfer in the vicinity of the interface. Therefore, better modeling of the metal−GNR interface is needed to accurately predict GNR FET scaling.[480,481] GNR width will also play an important role in determining the scalability of GNR FETs (narrower GNRs have higher effective mass and are less susceptible to source−drain tunneling).[66] Furthermore, it will be important to computationally quantify the tolerable magnitude of edge roughness as a function of GNR width to improve GNR FET performance. A synergistic combination of computational modeling and experimental characterization is required, but currently, comprehensive experimental device studies are lacking. For instance, relatively few experimental studies exploit nondestructive techniques such as Raman and X-ray photoelectron (XPS) spectroscopies to improve the understanding of metal−GNR interfacial properties such as doping, adhesion, strain, heat dissipation, *etc.*[371,482,483] Thankfully, the wealth of literature from graphene-, 2D materials-, and CNT-electronics could provide the necessary guidance in this regard.[484,485]

CONCLUSION

We conclude this Review with a message of cautious optimism. In agreement with the IRDS, we affirm that GNRs are promising candidates in future CMOS technologies and breakthrough quantum information sciences but are currently held back by the aforementioned materials science and integration challenges. A decade ago, the field of GNR electronics was plagued by the inability to achieve GNRs with sub-10 nm widths and atomically smooth edges, casting doubts on the feasibility of GNR-based technologies.[289] However, the field has evolved substantially since then, and promising routes for synthesizing narrow GNRs with smooth edges have been developed, including bottom-up organic synthesis, CVD on Ge, and lateral heteroepitaxy. The characterization of the GNRs produced *via* these techniques has somewhat lagged rapid developments in synthesis, and many fundamental questions remain. Importantly, how much edge roughness is present in these GNRs and how much can be tolerated in FETs, depending on the application? What are the intrinsic band gaps of the GNRs and how do these band gaps change in the presence of surrounding media (*e.g.*, because of dielectric screening effects)? How do GNR edge terminations change upon exposure to ambient conditions and/or during processing, and how do these factors influence transport properties? It is critical to answer these questions with the help of theory and experiments to scope out the potential applications of GNRs synthesized by different techniques.

Next, the field needs to move beyond the synthesis and study of individual GNRs and find ways to produce arrays of monodisperse GNRs with well-controlled pitch, alignment, and placement, with an ultimate goal of realizing these arrays on technologically relevant platforms. Rising stars are bottom-up organic synthesis and in-plane heteroepitaxy, yet both have challenges with placement and alignment. Lithography in conjunction with edge-annealing could lead to substantial improvements in the edge roughness of top-down fabricated GNR arrays, but achieving precise control over width in sub-5 nm GNRs will still be problematic. Direct CVD GNR growth on Ge or Ge/Si mediated by seeds is another noteworthy advancement in this field due to its potential CMOS-compatibility and the rising popularity of seed-initiated synthesis within the 2D materials community.[486] However the scalable fabrication of sub-5 nm seeds is still a formidable challenge. Furthermore, the integration of GNRs into devices is largely unexplored and underoptimized due to an incomplete understanding of interface effects and challenges associated with integrating and identifying appropriate contact and dielectric materials. Here, we believe that exploration of covalently bonded graphene−GNR or Mo−GNR edge contacts, integrating top-gate high-k dielectrics such as Al_2O_3 or Y_2O_3, and encapsulation with h-BN are low-hanging fruit in the field that can lead to tremendous improvements in the performance of existing devices and spur further interest among device engineers. Lastly, unconventional device architectures and concepts could be further explored, including but not limited to tunnel FETs, spin FETs, monolithic 3D integration, and devices that harness quantum coherence. The fields of CNT and 2D materials electronics have advanced tremendously due to concerted efforts by a wide community of synthetic chemists, materials scientists, and device engineers in overcoming similar roadblocks. A synergistic effort in the field of GNR electronics by academic researchers in collaboration with partners in industry is therefore critical to facilitating the adoption of GNRs in mainstream technologies.

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Notes

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VOCABULARY

Armchair graphene nanoribbon (AGNR): Graphene nanoribbon with long-axis parallel to armchair crystallographic orientation and armchair edge topology. Graphene nanoribbons with armchair edge topology exhibit substantial width-tunable band gaps. The armchair crystallographic direction of the graphene lattice is parallel to C−C bonds; **Zigzag graphene nanoribbon (ZGNR)**: Graphene nanoribbon with long-axis parallel to zigzag crystallographic orientation and zigzag edge topology. The zigzag crystallographic direction of the graphene lattice is 30° from C−C bond orientation; **Pitch**: Spacing between two aligned nanoribbons in a periodic array. Array nanoribbon field-effect-transistors need identical pitches to exhibit identical electronic characteristics; **On/off ratio**: Ratio of transistor drain currents in "on" and "off" states, characterizing the extent to which gate can modulate the current within the channel. On/off ratio is fundamentally dependent on the band gap of the channel material; **Carrier mobility**: The swiftness with which a charge travels in a material in response to a small, externally electric field. In long-channel devices, generally, higher carrier mobility leads to faster devices with higher current density; **Contact length**: The length over which contact metal and the semiconducting channel physically overlap. Generally, increased contact length leads to reduced contact resistivity in top-contacted devices; **Transfer length**: Distance over which $1 - e^{-1}$ of the total current is transferred from the contact metal to the semiconducting channel (where e is the natural number, also termed Euler's number). Transfer length characterizes the strength of coupling between the contact and the channel, and smaller transfer length indicates better coupling and therefore lower contact resistance

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