

Anodic oxidations: Excellent process durability and surface passivation for high efficiency silicon solar cells

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ABSTRACT

We investigate the versatility of anodically grown silicon dioxide (SiO₂) films in the context of process durability and exceptional surface passivation for high efficiency (> 23%) silicon solar cell architectures. We show that a room temperature anodic oxidation can achieve a thickness of ~70 nm within ~30 min, comparable to the growth rate of a thermal oxide at 1000 °C. We demonstrate that anodic SiO₂ films can mask against wet chemical silicon etching and high temperature phosphorus diffusions, thereby permitting a low thermal budget method to form patterned structures. We investigate the saturation current density J_0 of anodic SiO₂/silicon nitride stacks on phosphorus diffused and undiffused silicon and show that a J_0 of < 10 fA cm⁻² can be achieved in both cases. Finally, to showcase the anodic SiO₂ films on a device level, we employed the anodic SiO₂/silicon nitride stack to passivate the rear surface of an interdigitated back contact solar cell, achieving an efficiency of 23.8%.

1. Introduction

The development of versatile dielectric coatings is of great interest for photovoltaics, especially as the industry is seeking methods to boost the efficiency of solar cells while maintaining or even reducing manufacturing costs. Specifically, thermal silicon dioxide (SiO₂) is one example where a single dielectric film can be extremely versatile. In particular, thermal SiO₂ is used to electrically passivate the silicon surface [1,2], act as a barrier against wet chemical etching and thermal diffusions [3,4], mitigate potential induced degradation [5], insulate conducting layers from each other, and be applied as a passivated contact [6]. However, thermal oxidations require very high temperatures (~1000 °C) and long oxidation times (i.e. > 30 min), which detracts from their benefits. The high temperatures pose a risk of permanently degrading the bulk minority carrier lifetime and the high thermal budget can be expensive for commercial solar cells. For these reasons, there has been research on developing alternative approaches of growing SiO₂ that retain the same versatile qualities of thermal SiO₂, but which are grown at much lower temperatures [7]. Anodisation of silicon to grow silicon dioxide at room temperature is one promising

approach for PV applications [8,9].

Anodisation is a simple process whereby silicon wafers are immersed in an electrolyte (e.g. nitric acid) and a positive voltage is applied to the wafer relative to a counter electrode (e.g. a platinum wire) [10]. When a voltage is applied, oxygen-containing species (H₂O, O₂⁻, OH⁻) in the solution are forced to the positively biased silicon wafer where they oxidise the silicon surface and form a silicon dioxide film. Without the applied voltage, the formation of silicon dioxide is very slow and the thickness of the film cannot be controlled. Anodisation of silicon can be carried out under constant potential or constant current, each having their advantages and disadvantages. Under constant current operation, the voltage typically increases with oxide thickness, and in some cases can exceed 100 V [11]. This type of oxidation can form very thick oxides (> 100 nm), but is generally quite aggressive and thus susceptible to pit/defect formation [10]. Under constant potential operation, the current typically decreases as the oxide thickness increases. Although the oxidation rate is much slower under constant potential, the oxidation process is safer to operate. One could also speculate that a less aggressive oxidation in this case would also limit the pit/defect formation.

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Compared to thermal oxides, the properties of anodic oxide films are generally much poorer. For example, the density of the oxide is lower, the film is nonstoichiometric, the electrical resistance is lower (i.e. “leaky” in the context of metal-oxide-silicon devices), the dielectric constant is higher and the anodic oxides possess a much higher charge ($\sim 10^{12} \text{ cm}^{-2}$) and interface defect density D_{it} ($> 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$) [10]. In recent times however, there has been advancements in the development of anodic oxide films towards excellent surface passivation. Grant et al., examined the surface recombination velocity (S) of anodically grown SiO_2 post annealing in oxygen and forming gas at 400°C , and achieved an S of less than 40 cm s^{-1} (at $\Delta n = 10^{14} \text{ cm}^{-3}$) [9,12,13], similar to that achieved by a thermal SiO_2 [1]. However, in contrast to thermal SiO_2 , which can achieve a low D_{it} of $\sim 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$ and a low charge density of $\sim 10^{11} \text{ cm}^{-2}$ [14], the interface properties of the anodic oxide examined by Grant et al., revealed the low S primarily resulted from a higher charge density (i.e. $> 10^{12} \text{ cm}^{-2}$) rather than a low D_{it} [9,12]. To improve the interface properties, Cui et al. developed a light induced anodisation method, which permits single side anodic oxide growth, and was able to reduce the D_{it} of the oxide down to $6 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ [15,16]. Recently Grant et al., examined the benefits of capping the room temperature grown anodic SiO_2 film with a low-pressure chemical vapour deposition (LPCVD) silicon nitride (Si_3N_4) film [17]. When capped, the interface properties of the anodic SiO_2 film revealed a very low D_{it} and charge density of $\sim 2 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$ and $\sim 2 \times 10^{11} \text{ cm}^{-2}$ respectively, corresponding to an S of less than 3 cm s^{-1} (at $\Delta n = 10^{15} \text{ cm}^{-3}$) or a surface saturation current density of 3 fA cm^{-2} [17]. Despite the significant improvements in anodic oxide passivation over the past decade, the compatibility of the oxide in a solar cell fabrication process and the retention of surface passivation quality have yet to be demonstrated on a device level.

In this work we examine the versatility of room temperature grown anodic SiO_2 in the context of fabricating silicon solar cells. We examine the growth kinetics of the anodic SiO_2 film on diffused and undiffused silicon, and we assess their ability to mask against wet chemical silicon etching and high temperature phosphorus diffusions. We then examine the impact of the SiO_2 thickness on the saturation current density J_0 for diffused and undiffused silicon wafers. Finally, to demonstrate the robustness of the anodic SiO_2 films, we have fabricated a 23.8% efficient interdigitated back contact (IBC) solar cell employing the anodic SiO_2 layer to passivate the rear surface of an IBC cell.

2. Experimental Methods

Anodic oxidations were performed on (100) oriented n -type float-zone (FZ) silicon wafers with a diameter of 100 mm. For clarity, the thickness and resistivity of the wafers are described in the text. The wafers received an HF:HNO_3 (1:10) etch for 3 min to remove saw damage from their surfaces and were subsequently cleaved in half unless otherwise specified. The cleaved samples were then RCA cleaned using the standard procedure as outlined by Kern et al. [18], and etched in a 5% HF solution to remove the wet chemical oxide grown during the cleaning procedure.

Thermal diffusion of selected samples was performed in a Tempress 5-inch quartz tube furnace. In order to achieve a sheet resistance of $100 \pm 20 \Omega/\text{sq}$, phosphorus diffusions were conducted at 850°C for 20 min while the boron diffusions were performed at 890°C for 80 min. Following the thermal diffusions, the phosphosilicate and borosilicate glasses were removed in 5% HF. The diffused samples were subsequently RCA cleaned and given a final 5% HF dip prior to anodisation.

Anodic oxidations were performed by applying a +30 V bias across a silicon wafer and platinum wire electrode immersed in a 20% HNO_3 solution (at room temperature), where the silicon wafer was held at the higher potential. In order to connect the silicon sample electrically via an alligator clip, the top half was not immersed in the HNO_3 , meaning only half of each sample was anodically oxidised. Unless otherwise

specified, anodic oxidations were performed for 30 min.

Following the anodic oxidations, selected samples were air dried and then loaded into an LPCVD furnace. The Si_3N_4 deposition was performed at 780°C for 18 min yielding a nitride thickness of $\sim 100 \text{ nm}$. The thickness of the anodic SiO_2 and Si_3N_4 films were subsequently measured using a Filmetrics F20-UV thin-film analyser system.

Minority carrier lifetime measurements were performed using a Sinton WCT-120 PC lifetime tester under transient photoconductance decay (PCD) mode [19], and uncalibrated photoluminescence images were obtained using a BT Imaging LIS-R1 system [20]. PL images were acquired with excitation by a laser diode array with a wavelength of 808 nm. A $\pm 5\%$ uncertainty in the lifetime measurements was assumed for each dataset [21].

3. Results & discussion

3.1. Oxidation growth rate on diffused and undiffused silicon surfaces

Under constant potential, the oxidation kinetics during anodisation can exhibit substantially different growth rates depending on the electrolyte (composition, concentration and temperature), silicon material (type and doping concentration), applied voltage and illumination intensity [10,22]. For the purpose of this study, we fix the voltage at 30 V, we use a 20% HNO_3 solution as the electrolyte and the illumination intensity is determined by the fluorescent light housed in the fumehood, consistent with previous work [12,17]. Our focus is to understand how the silicon material properties influence the oxidation kinetics and how this might be useful in the context of silicon solar cells (i.e. masking purposes and/or surface passivation).

Fig. 1a plots the oxide thickness versus time for undiffused and diffused silicon grown at room temperature. For undiffused silicon, the increase in oxide thickness $d(t)$ with oxidation time can be expressed as a parabolic [10,23];

$$d(t) = d_0 + a \cdot \sqrt{t} \quad (1)$$

where a corresponds to the anionic properties of the oxide layer. For the purpose of this discussion we assume an initial oxide thickness of $d_0 = 0 \text{ nm}$. By fitting Eq. (1) to the undiffused data in Fig. 1a, we achieve an excellent fit when $a = 2.25$, which after taking the derivative of Eq. 1, corresponds to an oxidation rate of 1 nm/min at $t = 1 \text{ min}$ and 0.15 nm/min at $t = 60 \text{ min}$. To understand why the oxidation rate is relatively slow on undiffused c-Si, we must first understand the basic kinetics during anodisation of c-Si.

The growth of silicon dioxide on silicon requires the diffusion and/or drift of oxygen species (anions) through the oxide film, i.e. ionic current. Considering that our oxidations are performed at room temperature, one could assume that diffusion of oxygen-containing anions is too slow to account for the oxide growth rates observed in this work [10]. In this regard, inward movement/migration of the oxygen source must be field-assisted, which is primarily determined by the field strength (i.e. voltage across the oxide) [10]. Assuming the measured current during anodisation is ionic, and that its magnitude depends on the field strength across the oxide, Fig. 1b (red squares) indicates that the field strength in the undiffused c-Si case must be relatively weak, evident by the low ionic current ($0.3\text{--}0.4 \text{ mA cm}^{-2}$) measured during anodisation. Notably, we do not attribute the low ionic current to a high contact resistance between the metal clip and silicon wafer, because in our previous work it was demonstrated that an increase in voltage from 30V to 60V did not increase the anodisation current, indicating the current is limited by the oxidation kinetics and not the contact resistance [24].

When anodisation is performed on diffused silicon wafers, we see a large increase in the oxide thickness after 1 min, where a thickness of $\sim 35 \text{ nm}$ has been measured, as shown by the green circles in Fig. 1a. To gain further insight into the growth kinetics under these conditions, Fig. 1b plots the corresponding current profile of a phosphorus diffused

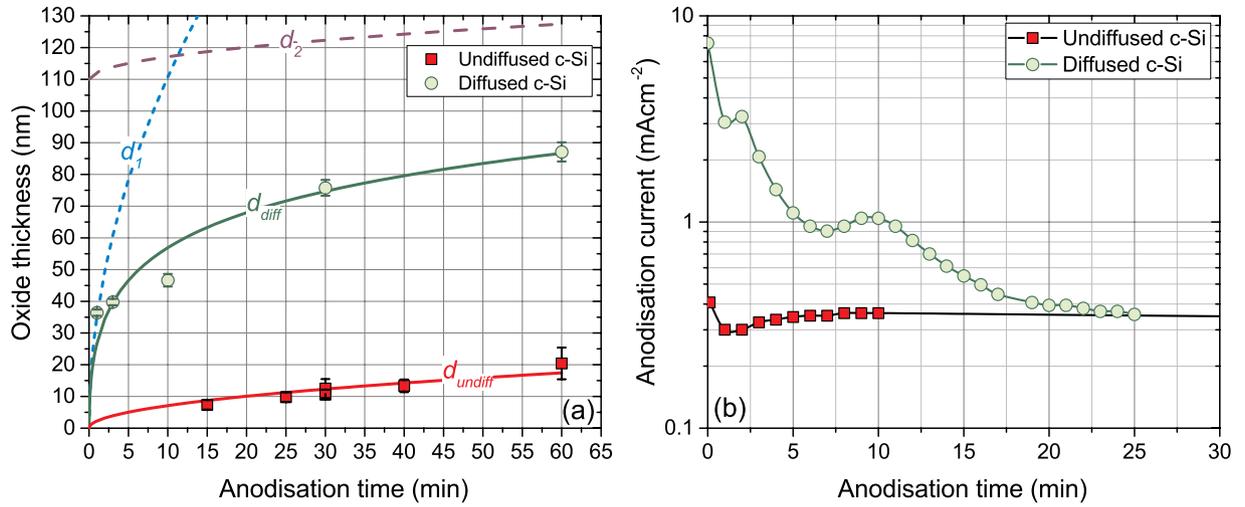


Fig. 1. (a) Oxide thickness versus anodisation time on undiffused *n*-type silicon (red squares) and phosphorus diffused ($\sim 100 \Omega/\text{sq}$) silicon (green circles). d_{undiff} (red line) and d_{diff} (green line) correspond to parabolic trends which approximate the oxide thickness as a function of anodisation time for undiffused and diffused silicon respectively. In the case for d_{diff} , the inverse sum of two parabolic trends d_1 (dashed blue line) and d_2 (dashed purple line) was required to model the oxide thickness on diffused silicon. (b) Current density versus oxidation time for undiffused (red squares) and phosphorus diffused (green circles) silicon samples. All oxidations were performed at room temperature. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

($\sim 100 \Omega/\text{sq}$) silicon wafer during anodisation. At time $t = 0$ min, the current is very high relative to undiffused c-Si (8 mA cm^{-2}), and this rapidly declines over the first few minutes. This behaviour indicates the field strength across the growing oxide must be higher than in the undiffused case, however the cause for this enhancement is not well understood at this time. Nevertheless, we can still draw some meaningful insight regarding the potential mechanism(s) giving rise to the higher oxidation rates on diffused silicon. Firstly, the oxidation of silicon during anodisation requires a reaction with a hole from the valance band at the silicon surface [10], meaning the mechanism by which holes can react at the silicon surface has been enhanced, e.g. accumulation of holes at the c-Si surface or injection of electrons into the conduction band via reactions with the electrolyte. Secondly, it is also possible that surface states arising from highly diffused phosphorus and boron (not shown) surfaces enhance one, or both of these mechanisms via generation-recombination centres [10,25].

For $t > 10$ min, the oxidation rate appears to slow rapidly, i.e. from $\sim 10 \text{ nm/min}$ at $t = 1$ min to 1.5 nm/min at $t = 10$ min. Thus contrary to undiffused silicon, where the oxide thickness follows a steady parabolic trend with time, oxidation on diffused silicon does not behave in a similar manner. Therefore in order to accurately fit the data for diffused c-Si in Fig. 1a, it is necessary to treat the oxidation growth as a two-step process, i.e. two parabolic trends. In the initial stages of oxidation, the oxide thickness d_1 can be expressed as,

$$d_1(t) = 35 \cdot \sqrt{t} \quad (\text{with } d_0 = 0 \text{ nm}) \quad (2)$$

however after some minutes of oxidation, the cause for this exceptionally high growth rate $\gg 1 \text{ nm/min}$, transitions to a much slower one ($< 1 \text{ nm/min}$), i.e. equivalent to that for undiffused silicon,

$$d_2(t) = 110 + 2.25 \cdot \sqrt{t} \quad (3)$$

having established fitting parameters for each of the parabolic expressions, d_1 and d_2 must be inversely summed to calculate the oxide thickness with time for diffused c-Si, where;

$$\frac{1}{d_{diff}} = \frac{1}{d_1} + \frac{1}{d_2} \text{ yields,} \\ d_{diff}(t) = \frac{2.25 \cdot 35 \cdot t + 35 \cdot 110 \cdot \sqrt{t}}{\sqrt{t}(2.25 + 35) + 110} \quad (4)$$

the expression derived in Eq. (4) allows us to predict the oxidation thickness and rate on diffused silicon for the conditions described in

this work, however we do expect this trend to vary depending on material properties and anodic oxidation conditions (voltage, electrolyte, temperature, etc). Thus, while fitting the data using the inverse sum of two parabolic expressions is robust, individual fitting parameters will need to be determined using experimental data corresponding to specific conditions in which the anodic oxidation is being performed.

From our examination of anodic oxide growth on diffused and undiffused c-Si, it is clear a wide range of oxide thicknesses under well controlled conditions can be achieved. We now assess their robustness in the context of masking against thermal diffusions and wet chemical etching for PV applications.

3.2. Masking durability of anodically grown SiO_2 films

In this work we examine whether anodically grown silicon dioxide films can mask against phosphorus during a thermal diffusion process, which could be useful in the context of high efficiency cell designs, e.g. IBC solar cells, where masking is required to protect locally diffused regions. Notably, we have not examined masking against boron because, as elucidated in Ref. [4], boron diffuses much slower than phosphorus through an SiO_2 film, thus the barrier oxides developed in this work should also be applicable to masking against boron.

Firstly, an $FZ > 100 \Omega \text{ cm}$ *n*-type wafer was subject to a boron diffusion, yielding a sheet resistance of $\sim 100 \Omega/\text{sq}$ as outlined in the Experimental Methods section. Following the boron diffusion, half of the boron diffused sample was anodically oxidised for 30 min resulting in an oxide thickness of $\sim 70 \text{ nm}$. Subsequently, the sample (half oxidised and half bare c-Si) was subject to a phosphorus diffusion in a quartz tube furnace at $850 \text{ }^\circ\text{C}$ for 20 min. Following the phosphorus diffusion, the anodic SiO_2 film and phosphosilicate glass were removed in 10% HF. To determine if phosphorus did penetrate the anodic oxide film during the diffusion step, an electrochemical capacitance voltage (ECV) technique was used to measure the boron and phosphorus concentrations in the silicon wafer. Fig. 2 plots the results.

From Fig. 2a, which plots the dopant concentration of an unprotected sample, the ECV measurement detected a high concentration of phosphorus and boron in the near surface region of the sample. However in Fig. 2b, which plots the dopant concentration for a sample protected by a thick (70–80 nm) anodic SiO_2 film, the ECV measurement could only detect boron. Our ECV results therefore indicate the anodic SiO_2 film did prevent phosphorus from diffusing through the

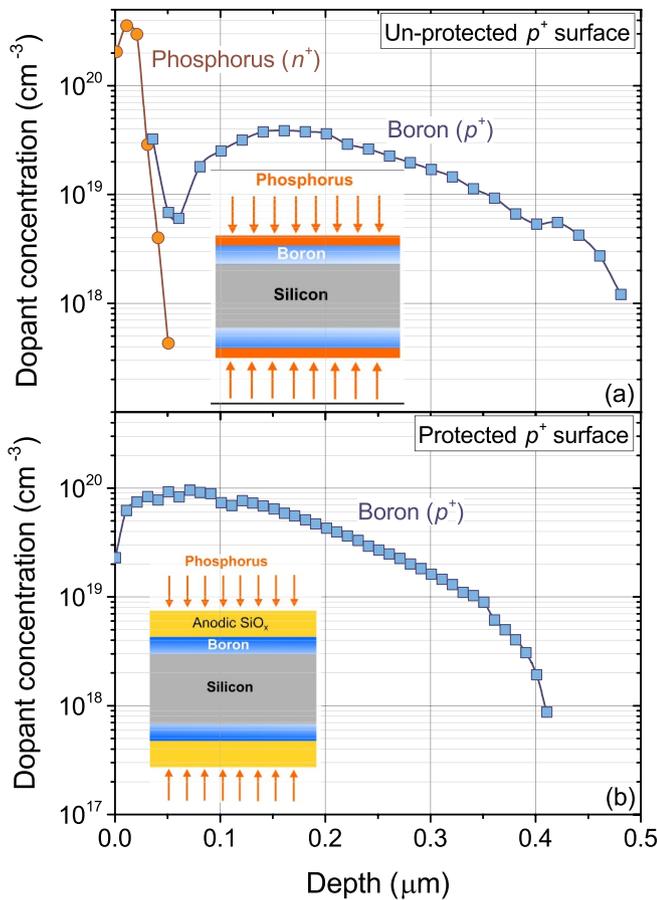


Fig. 2. ECV doping profile measurements of a boron diffused c-Si sample (a) un-protected and (b) protected by a thick anodic oxide film (~70 nm) during a subsequent phosphorus diffusion process. Blue squares and orange circles correspond to boron and phosphorus dopants respectively. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

film into the silicon sample. Notably, although the oxides were initially grown at room temperature, they were subject to high temperatures before, and during the thermal diffusion process, meaning the anodic oxides become more like thermal oxides, whereby effusion of OH⁻ from the SiO₂ network results [22]. In this regard, it should be expected that thick anodic SiO₂ films form a good barrier against impurity

diffusion during thermal processing.

Another benefit of thermally grown SiO₂ films is their ability to mask against wet chemical processing. This is particularly advantageous when localised areas of a solar cell require etching, e.g. to remove diffused regions from the front/rear or process locally diffused regions (PERC, IBC). In most cases, etching diffused regions can be as short as several minutes. In this work, we investigate the masking durability of anodically grown SiO₂ films when subjected to a silicon etch solution.

Firstly, an FZ > 100 Ω cm n-type wafer was subjected to a phosphorus diffusion, yielding a sheet resistance of ~100 Ω/sq as outlined in the Experimental Methods section. Following the phosphorus diffusion, half of the phosphorus diffused sample was anodically oxidised for 30 min resulting in an oxide thickness of ~70 nm. Prior to subjecting the sample to a wet chemical etch, the effective lifetime was measured, along with its spatial uniformity using PL, Fig. 3 depicts the results.

Fig. 3a shows a PL image of an anodically oxidised sample prior to immersing in a hot (80–90 °C) tetramethylammonium hydroxide (TMAH) solution. In this case the diffusion provides sufficient surface passivation to yield a PL signal. It is important to note that the anodic oxide (protected region in Fig. 3a) has not been thermally treated, and thus is not providing a notable level of surface passivation. In this case, the higher PL intensity arising from the anodic oxide results because defect states within the oxide layer are luminescing at similar wavelengths to the silicon, and does not result from additional surface passivation [10]. Therefore any reduction in the effective lifetime would imply the diffusion has been etched.

In order to quantify how well the oxide protects the diffusion during wet chemical etching, we measure both the effective lifetime and PL intensity. Etching the sample for 12 min in TMAH allows sufficient time to remove the diffusion from the unprotected part of the sample, which is evident by the very low PL signal shown in Fig. 3b, indicating that all passivation resulting from the diffusion has been lost. Further etching of the sample does not change the behaviour (PL and lifetime signal) of the unprotected region. In contrast, etching the protected region for 12 or even 36 min does not significantly alter the PL signal and effective lifetime, indicating that the surface passivation remains unchanged and hence the diffusion remains intact. However, after thoroughly rinsing the sample in DI water and storing in a petri-dish for 24 h, the silicon surface underwent some surface modifications whereby the diffusion has been slightly etched, evident by the change in PL uniformity and effective lifetime measurement. This suggests that although the sample was thoroughly rinsed prior to storing the sample, it still contained TMAH residue within the SiO₂ film.

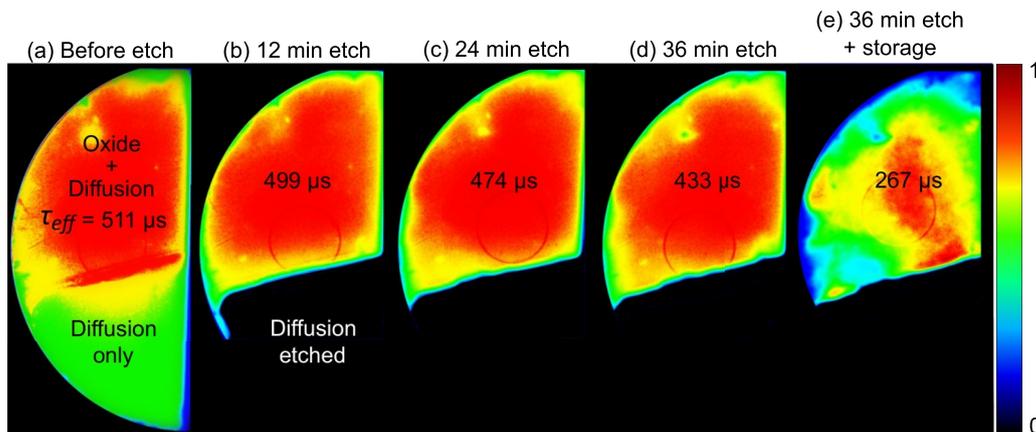


Fig. 3. Normalised PL images of a phosphorus diffused (~100 Ω/sq) c-Si 100 mm diameter wafer (halved) that was subsequently anodically oxidised for 30 min at room temperature. Only the top half of the sample was oxidised. (a) before etching in TMAH, (b) after a 12 min etch in TMAH at 80–90 °C, (c) 24 min etch, (d) 36 min etch and (e) 36 min etch and subsequently stored overnight in a petri-dish. In (b) to (e) the bottom part of the wafer is still present, but appears black in the PL image due to excessive surface recombination. The etch rate of TMAH at 80–90 °C is ~1 μm/min.

3.3. Surface passivation of diffused and undiffused silicon surfaces

In our examination of anodically grown SiO_2 films thus far, we have focused on applications in which these oxides can be used to alleviate high temperature processing to form masking barriers during wet chemical etching and thermal diffusions. Here we examine the capability of anodic SiO_2 films to passivate the c-Si surface, and thus their permanent use in c-Si solar cells.

Fig. 4 plots the saturation current density J_0 versus oxide thickness after the deposition of LPCVD Si_3N_4 . In this case, the addition of the Si_3N_4 layer was necessary to achieve a very high level of surface passivation and to mitigate moisture ingress, as demonstrated in Ref. [17]. Notably, the surface passivation of the anodic oxide partly benefits from the high temperature ($\sim 780^\circ\text{C}$) LPCVD deposition, but as demonstrated previously, a 400°C without the Si_3N_4 layer can also result in good surface passivation [9,12,13]. Another benefit of using LPCVD Si_3N_4 on top of the anodic SiO_2 was to enable a direct substitution for the thermal SiO_2 /LPCVD Si_3N_4 stack in our existing IBC fabrication process, where previously we had achieved a certified efficiency of 24.4% [26]. In Fig. 4, the J_0 was determined from the slope of the inverse lifetime using the method of Kane and Swanson [27], which was measured by the PCD method [28]. The vertical error bars in Fig. 4 represent the uncertainty in J_0 when accounting for variations in the bulk lifetime (e.g. when intrinsic defect recombination is more dominant than Auger), as measured by the light-enhanced HF passivation technique [29,30]. The horizontal error bars represent the spatial variation in oxide thickness across each sample.

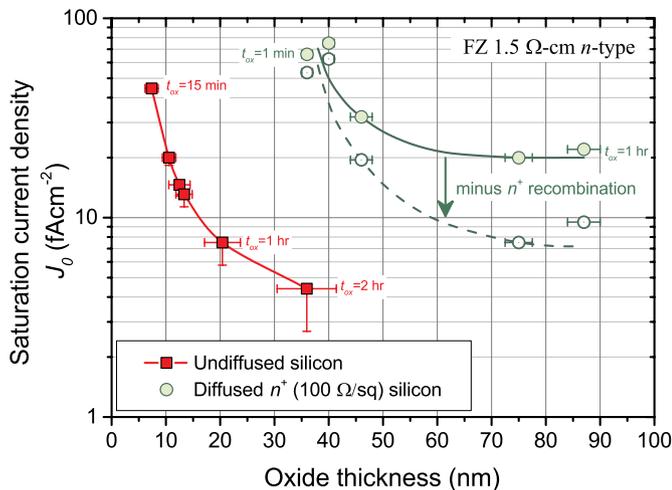


Fig. 4. J_0 versus oxide thickness after capping the anodic oxide films with 100 nm of Si_3N_4 . The red squares and green circles correspond to undiffused and diffused c-Si respectively. ' t_{ox} ' represents the oxidation time. The 'minus n^+ recombination' refers to the case when the emitter J_0 has been removed from the total J_0 . The base material was 200 μm FZ 1.5 $\Omega\text{-cm}$ n -type. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

Fig. 4 demonstrates that for both diffused and undiffused silicon samples, the J_0 decreases with increasing oxide thickness. In the case for undiffused silicon (red squares), the J_0 decreases from 45 to 4.5 fA cm^{-2} for an oxide thickness of 7 and 36 nm respectively, while for diffused silicon (green circles), the J_0 decreases from 70 to 20 fA cm^{-2} for an oxide thickness of ~ 40 and > 70 nm respectively. The absolute oxide thickness therefore does not appear to govern the level of surface passivation, but rather the oxidation time. In a previous publication (on undiffused c-Si) it was shown that as the oxide thickness

increased (with increasing oxidation time), the midgap D_{it} reduced from $\sim 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ (at 7 nm) to $\sim 2 \times 10^{10}$ (> 20 nm) and a similar trend was observed for the effective charge Q_{eff} and hole capture cross-section σ_p [17]. Based on these findings for undiffused c-Si, we can only speculate that the same passivation mechanisms are occurring for diffused c-Si (e.g. increasing oxidation time reduces D_{it} , Q_{eff} and σ_p).

Finally, the higher J_0 values measured on the diffused wafer could in part, be attributed to additional recombination occurring in the diffused region. In this case we can expect this additional recombination to be as high as 10–15 fA cm^{-2} when modelled using EDNA 2 (assuming no SRH at the surface or in the emitter) [31]. Taking this into account, i.e. by subtracting the n^+ recombination from the total recombination, the diffused and un-diffused surfaces attain similar levels of surface passivation, as demonstrated in Fig. 4 (compare the red line to the dashed green line), after similar oxidation times.

3.4. Integration of anodic oxide passivation for rear contact solar cells

To demonstrate the compatibility of our anodic oxidation process for high efficiency solar cells, we utilised the anodic SiO_2 /LPCVD Si_3N_4 stack demonstrated in Fig. 4, and applied it to passivate the rear surface of our IBC solar cells. In this fabrication sequence, the anodic oxides were not required to provide masking during thermal diffusions and wet chemical etching, however as demonstrated above, room temperature anodic oxidations would have been a suitable substitution for high temperature thermal SiO_2 masking.

For clarity we will briefly describe the IBC cell design, however for a more detailed description, the reader is referred to Ref. [26]. Anodic oxide passivated IBC solar cells (4 cm^2) were fabricated on a 4 inch FZ 100 $\Omega\text{-cm}$ n -type wafers with a final cell thickness of $\sim 200 \mu\text{m}$. The front surface was randomly textured and passivated by ~ 70 nm of PECVD $a:\text{SiN}_x:\text{H}$ (single ARC layer in this case). The rear surface underwent a slight modification to that presented in Ref. [26] where (i) the undiffused regions were replaced by a light phosphorus diffusion ($\sim 600 \Omega/\text{sq}$) to mitigate bulk lifetime degradation, making up 88% of the rear surface and (ii) the boron diffused regions (hole collecting contact) were reduced to 10% (originally 64%) of the total cell area. The metallised contact regions remain unchanged. The rear surface was passivated by a ~ 70 nm anodic SiO_2 /100 nm LPCVD Si_3N_4 stack (analogous to step 10 in Ref. [26]). In this case, the anodic oxidation did not add an additional processing step, but rather it replaced the high temperature thermal oxidation used in our 24.4% IBC cell [26].

Fig. 5a plots the effective lifetime on the wafer immediately prior to rear contact opening and metallisation, whereby a total J_0 of 20 fA cm^{-2} was determined. Assuming the PECVD $a:\text{SiN}_x:\text{H}$ front surface layer contributes $\sim 5 \text{ fA cm}^{-2}$, as demonstrated in Ref. [26], implies that the J_0 resulting from the anodic SiO_2 /LPCVD Si_3N_4 stack is, at worst, $\sim 15 \text{ fA cm}^{-2}$, consistent with the trends shown in Fig. 4. The high lifetime shown in Fig. 5a indicates that our IBC process does not significantly degrade the bulk lifetime, however for high resistivity ($> 100 \Omega\text{-cm}$) silicon, one should expect much higher lifetimes as demonstrated in Refs. [33,34]. In this case, it is difficult to assess whether the lifetime is still limited by thermally active bulk defects inherently incorporated during ingot growth [35–37], or whether the wafer has been slightly contaminated. Nevertheless, the slightly low bulk lifetime will not have a significant influence on the cell efficiency relative to our 24.4% baseline.

Fig. 5b plots the light I–V measurement of our anodic oxide passivated IBC solar cell. As a first trial, the measured efficiency of 23.8% is extremely promising and demonstrates the robustness and compatibility of anodic SiO_2 films for high efficiency solar cell designs. Table 1 compares I–V measurements from this work with those of our 24.4% IBC cell.

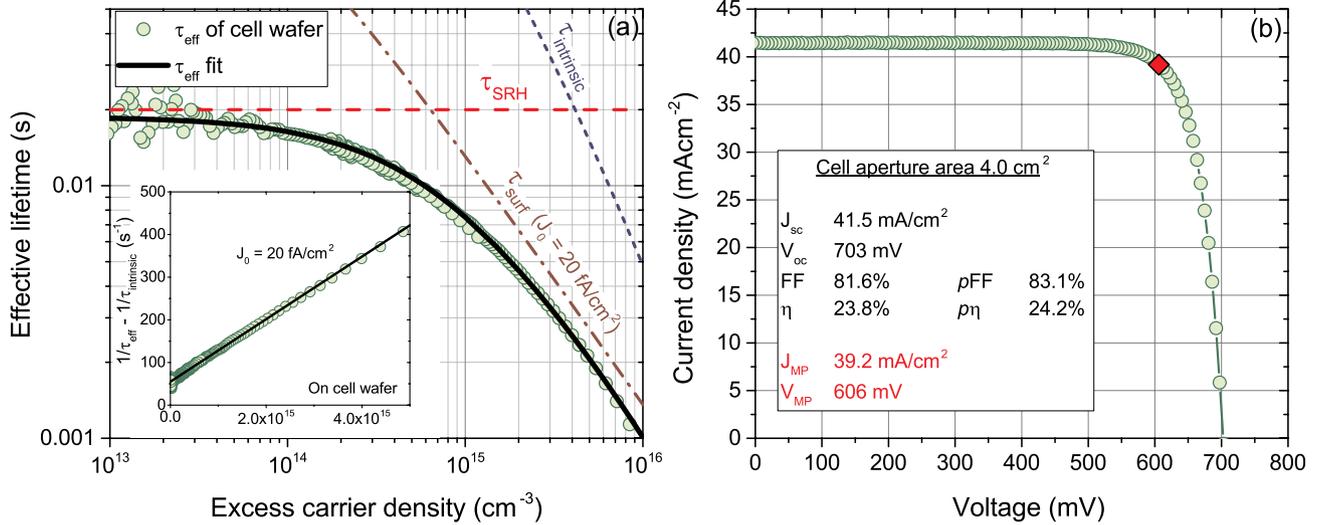


Fig. 5. (a) Effective lifetime measurement of the IBC cell wafer immediately prior to rear contact opening and metallisation. The insert of Fig. 5(a) plots the inverted residual lifetime in order to accurately extract the total J_0 of the cell wafer, which includes front and rear recombination. The intrinsic lifetime limit $\tau_{\text{intrinsic}}$ was calculated from Ref. [32]. (b) I-V measurement of our first IBC solar cell featuring rear side anodic $\text{SiO}_2/\text{Si}_3\text{N}_4$ passivation.

Table 1

Comparison of light I-V parameters for our anodic oxide passivated IBC cell and our 24.4% IBC cell baseline.

	Anodic oxide IBC cell	Baseline IBC cell ^a [26]
V_{oc} (mV)	703	703 ± 3.5
J_{sc} ($\text{mA}\cdot\text{cm}^{-2}$)	41.5	42.0 ± 1.0
Fill Factor (%)	81.6	82.7 ± 0.8
Efficiency (%)	23.8	24.4 ± 0.7
Pseudo-Fill Factor (%)	83.1	–
Pseudo-Efficiency (%)	24.2	–
R_{series} ($\Omega\cdot\text{cm}^2$)	0.3	0.2

^a The uncertainty in the measured cell parameters were obtained during the independent certification of our baseline IBC solar cell.

From Table 1 it can be seen that the open circuit voltage (V_{oc}), short circuit current (J_{sc}) and efficiency of the two cells are the same within the uncertainty of the measurements, as evident by the error margins for the certified measurement. The drop in fill factor (FF) is largely due to higher series resistance (R_s), which can simply be attributed to process variability, as experienced from our batch to batch variations (not shown). The similarity in cell performance therefore supports the robustness and quality of the anodic oxidation fabrication steps.

We note, however, that there are several small differences in the physical attributes of the cells. For completeness we perform optical and electrical simulations, using SunSolve [38,39] and Quokka 2 [40] respectively, to evaluate how those differences affect the cell performance, thereby providing a superior comparison between the two cells. Details of the optical and electrical simulations can be found in the Appendix. The differences are now discussed:

3.4.1. Optical differences

On the front surface, the baseline cell had a double antireflective coating consisting of an 80 nm PECVD silicon oxide film on top of an 75 nm $\alpha\text{-SiN}_x\text{:H}$ layer, while the anodic oxide cell had a single layer antireflective coating (SLARC) consisting of an ~ 70 nm thick $\alpha\text{-SiN}_x\text{:H}$ film. On the rear surface, the baseline cell had a 30 nm thick thermal SiO_2 film, while the anodic oxide cell had a ~ 70 nm thick anodically grown SiO_2 film. Both SiO_2 films were capped by a ~ 100 nm Si_3N_4 layer.

Our optical simulations indicate these differences would reduce the photogeneration current (J_{gen}) in the anodic oxide IBC cell by 0.26 mA cm^{-2} .

3.4.2. Electrical differences

The base resistivity was increased from $1.5 \Omega \text{ cm}$ (baseline cell) to $100 \Omega \text{ cm}$ (anodic oxide cell), and correspondingly, we measured an increase in the bulk lifetime from 5 ms to 20 ms. The total J_0 of the anodic oxide IBC cell increased from 20 fA cm^{-2} (as shown in Fig. 5a) to $\sim 40 \text{ fA cm}^{-2}$. This increase in J_0 indicates that some surface passivation had been lost during the metallisation process, and in this case, we have assumed this loss to be at the rear. Finally, a higher series resistance of $0.3 \Omega \text{ cm}^2$ was measured on the anodic oxide IBC cell compared to $0.2 \Omega \text{ cm}^2$ measured on the baseline.

Our electrical simulations (which include our J_{gen} simulations) indicate there is little difference in the V_{oc} and J_{sc} between the two cells, however the FF does decrease by 1.1% in the case for the anodic oxide IBC cell. Table 2 presents the simulated IV parameters of each IBC cell.

Table 2

Simulated light I-V parameters of the baseline and anodic oxide passivated IBC solar cells.

	Anodic oxide IBC cell	Baseline IBC cell [26]
V_{oc} (mV)	704	704
J_{sc} ($\text{mA}\cdot\text{cm}^{-2}$)	42.3	42.2
Fill Factor (%)	81.5	82.6
Efficiency (%)	24.3	24.5

The simulated IV parameters shown in Table 2 demonstrate the cells are equivalent to the measured values, within the accuracy of the experiment, thereby supporting the credibility of the simulations and our conclusions regarding the robustness of the anodic SiO_2 film. We note that, although within the accuracy of the experiment, possible reasons for the simulated J_{sc} being higher than the experimental J_{sc} of the anodic oxide IBC cell are:

1. The front textured surface is spatially imperfect.
2. The front J_0 is higher than measured on test samples.
3. A lower bulk lifetime than measured in Fig. 5a.
4. The estimates of the front thin film thicknesses are different to the actual film thicknesses, thereby yielding a higher reflectance.
5. The rear surface is slightly more absorbing than we have accounted for (due to a thinner SiO_2 film).
6. Slightly more free carrier absorption.

4. Conclusion

In this paper, we have examined the versatility and robustness of anodically grown silicon dioxide layers for high efficiency silicon solar cells. Compared to high temperature thermal oxidations, our room temperature grown anodic SiO₂ films have performed exceptionally well, demonstrating their ability to mask against wet chemical silicon etching, and high temperature phosphorus diffusions. The masking durability of the films was attributed to our ability to grow thick SiO₂ layers (> 70 nm), with a relatively short oxidation time (~30 min) comparable to a 1000 °C thermal oxidation. We investigated the J_0 of Si₃N₄ capped anodic SiO₂ films, and demonstrated the oxidation time, and not the oxide thickness, governs the level of surface passivation achieved on both diffused and undiffused c-Si. We also demonstrated that, after subtracting away recombination occurring in the diffused

region, the trends in J_0 with oxidation time are very similar on both diffused and undiffused c-Si, where a J_0 of less than 10 fA cm⁻² was achieved. Finally, to showcase the anodic SiO₂ films on a device level, we employed the anodic SiO₂/LPCVD Si₃N₄ stack to passivate the rear surface of an IBC solar cell, achieving an efficiency of 23.8%, thereby demonstrating that anodic SiO₂ films are compatible with high efficiency devices.

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Appendix

Photogeneration current density simulations of the IBC cells were performed using SunSolve, a sophisticated ray tracing program which accounts for front/rear surface reflection and absorption and non-ideal light trapping as a function of wavelength [38,39].

Our 3D device simulations were carried out using Quokka 2 [40]. Table A1 lists the key cell parameters used in these simulations, which have been determined from the device itself, or from monitor wafers co-processed through each of the relevant process steps.

Table A.1

Key properties for the 2 × 2 cm² baseline and anodic oxide passivated IBC solar cells used in our 3D device modelling.

Property	Anodic oxide IBC cell	Baseline IBC cell [26]
Cell thickness	200 μm	230 μm
Wafer resistivity	100 Ω cm	1.5 Ω cm
Bulk SRH lifetime (τ_n/τ_p)	2000 μs/20000 μs	5000 μs/5000 μs
Rear pitch	500 μm	500 μm
Emitter width	–	330 μm
Emitter (diameter/pitch)	36 μm/70 μm	–
BSF (diameter/pitch)	27 μm/70 μm	27 μm/70 μm
n contact (diameter/pitch)	7 μm/70 μm	7 μm/70 μm
p contact (diameter/pitch)	7 μm/70 μm	7 μm/70 μm
Emitter sheet (R/J_0)	120 Ω/□/60 fA cm ⁻²	166 Ω/□/36 fA cm ⁻²
BSF sheet (R/J_0)	30 Ω/□/130 fA cm ⁻²	19 Ω/□/190 fA cm ⁻²
Undiffused rear J_0	–	21 fA cm ⁻²
Light BSF rear (R/J_0)	600 Ω/□/35 fA cm ⁻²	–
Front surface J_0	5 fA cm ⁻²	5 fA cm ⁻²
n contact (J_0/ρ_c)	600 fA cm ⁻² /~10 ⁻⁵ Ωcm ²	280 fA cm ⁻² /~10 ⁻⁵ Ωcm ²
p contact (J_0/ρ_c)	1200 fA cm ⁻² /~1.5 × 10 ⁻⁵ Ωcm ²	810 fA cm ⁻² /~1.5 × 10 ⁻⁵ Ωcm ²
n finger/p finger width	134 μm/282 μm	134 μm/282 μm
Finger sheet resistance	6.3 mΩ/□	6.3 mΩ/□

For the purpose of our simulations, we have neglected edge recombination and therefore all the simulated parameters will be slightly higher than if edge recombination were included.

Declarations of interests

None.

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