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High-Fidelity TiN Processing Modes for Multigate Ge-Based Quantum Devices

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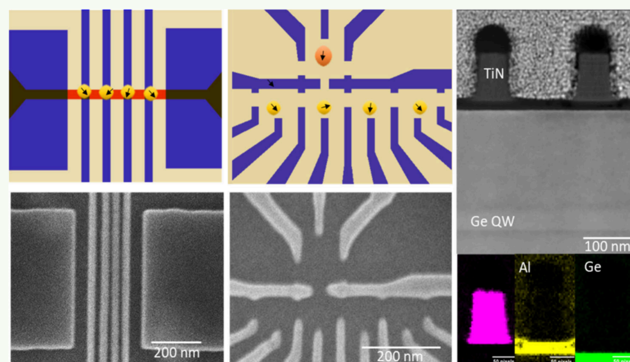
ABSTRACT: Charge or spin-qubits can be realized by using gate-defined quantum dots (QDs) in semiconductors in a similar fashion to the processes used in CMOS for conventional field-effect transistors or more recent fin FET technology. However, to realize a larger number of gate-defined qubits, multiples of gates with ultimately high resolution and fidelity are required. Electron beam lithography (EBL) offers flexible and tunable patterning of gate-defined spin-qubit devices for studying important quantum phenomena. While such devices are commonly realized by a positive resist process using metal lift-off, there are several clear limitations related to the resolution and the fidelity of patterning. Herein, we report a systematic study of an alternative TiN multigate definition approach based on the highest resolution hydrogen silsesquioxane (HSQ) EBL resist and all associated processing modes. The TiN gate arrays formed show excellent fidelity, dimensions down to 15 nm, various densities, and complexities. The processing modes developed were used to demonstrate applicability of this approach to forming multigate architectures for two types of spin-qubit devices prototypic to (i) NW/fin-type FETs and (ii) planar quantum well-type devices, both utilizing epi-grown Ge device layers on Si, where GeSn or Ge is the host material for the QDs.



KEYWORDS: *electron beam lithography, HSQ, TiN patterning, quantum devices*

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1. INTRODUCTION

There are several proposed platforms for realizing qubits, the basic units of quantum information processing, and to perform quantum computation.[1] While there has been great scientific progress and proof-of-concept demonstrations on all these platforms, to address the challenge of scalability, it makes sense to use all the machinery of traditional semiconductor integrated circuits, which also opens the possibility of integrating classical computing with quantum accelerators.[2,3] To this end, recent developments in the field of quantum device engineering have shown that charge or spin-qubits can be realized in gate-defined quantum dots in semiconductors in a similar fashion to state-of-the-art field-effect transistors (FETs).[4−7] In the past few years, Ge has progressed immensely from a conceptually new material for qubits to demonstrations of two-qubit logic and most recently the first demonstration of a four-qubit quantum processor.[8,9] Furthermore, the GeSn alloy is a material platform that carries the promise of highly desirable extreme mobility, low effective mass, and added optical control for the qubits operation. The ultimate realization of quantum circuits will require patterning processes with high-density gate structures at ultimately small widths and spacings between the neighboring structures to accommodate a large number of qubits.[10] The unique arrangement of gates and their high-resolution patterning allow for programmable and well-controlled interdot coupling and consequently high-fidelity spin−spin interactions as predicted by numerous theoretical studies.[11−13]

Before such conceptually new devices are mass produced, CMOS-compliant patterning processes can be employed to demonstrate the promised advantages. While extreme ultraviolet lithography (EUV) has been projected to reach ultimate resolution and fidelity for sub-10 nm CMOS technology modes,[14] electron beam lithography (EBL) is currently used widely for device prototyping of Si and Ge spin-qubit devices.[15] Due to the easily tunable patterning, gate defined quantum dots (QDs) with controllable localization and density in Si, SiGe, and Ge were realized to demonstrate quantum effects such as Coulomb blockade and spin exchange.[9,10] Most

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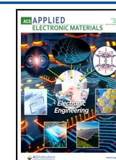

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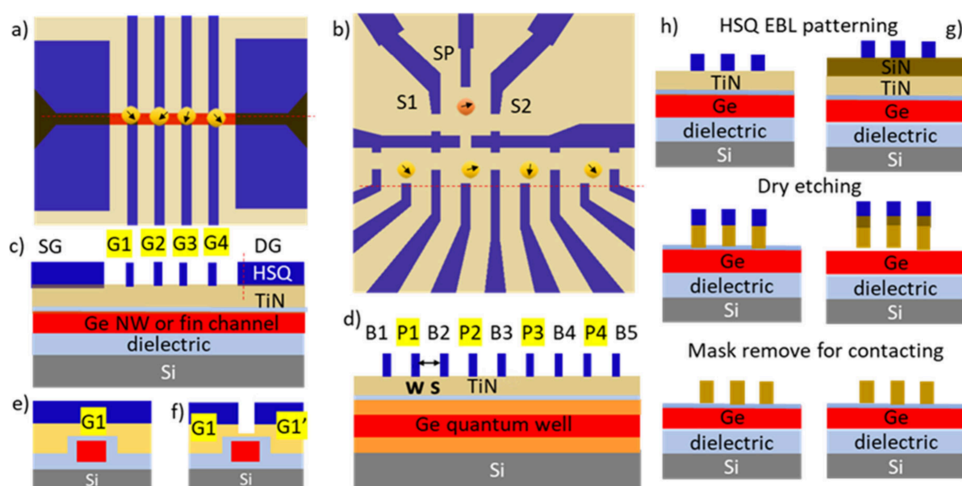

Figure 1. Schematics of the gate designs for gate-defined QDs (in yellow) using HSQ EBL processing for a) NW/fin FET devices and b) quantum well devices and the corresponding cross-sectional representations of the layers c) source gate (SG), QD defining gates (G1−G4) and drain gate (DG) and in d) barrier gates (B1−B5) and plunger gates (P1−P4). The representations in c) and d) are taken across the dotted lines. Shown also are the gates' width (W) and spacing (S) between the gates that are increased in the EBL design by 5 nm, starting at W = 15 nm and $S = 2 \times W$. Additionally, the quantum well device in b) depicts a sensor dot defined by gates S1, S2, and sensor plunger gate (SP). For the NW- or fin-type devices in a) the gates can be defined as e) π-gates and f) split gates, the latter doubling the total number of QDs. Summary of the total processing sequence for TiN gate definition using h) TMAH and g) salty NaOH HSQ developers; Ge is NW, fin, or QW.

of the demonstrated devices use metal gates including magnetic materials such as cobalt,[16] formed by lift-off process and defined in a positive poly(methyl methacrylate) (PMMA)-based EBL resist. While the PMMA EBL and lift-off processing modes are relatively well established, there are several clear limitations related to the density/smallest dimensions obtainable, the line-edge roughness, and the retention of metal between densely packed structures.[15] An alternative is the hydrogen silsesquioxane (HSQ), an inorganic resist, which is the resist of choice for high-resolution definition of structures with sub-10 nm dimensions,[17] including patterning of metallic structures such as Ag waveguides for plasmonic applications.[18] We have investigated the EBL HSQ process for epi-grown Ge-containing layers on Si substrates, demonstrating that moving from Si- into Ge-containing substrates comes with its own challenges, limiting resolution and fidelity of the line structures obtained.[19] Titanium nitride (TiN) gate technology has already been introduced in CMOS fabrication, capitalizing on the need for replacing poly-Si gates with metal gates integrated with high-k gate oxides on Si but also for other channel materials.[4,5] Separately, TiN on its own can be classified as a quantum material due to its superconducting and plasmonic properties.[20] Extending this EBL-based technology to TiN for patterning gate-defined QDs and ultimately qubits is a natural development that capitalizes on ultimately small dimensions, high fidelity, and low line-edge roughness of the HSQ defined structures.

Herein we present a systematic study of the processing modes for realization of multigate TiN line structures, patterned by HSQ EBL and subsequent reactive ion etching (RIE). The TiN processing modes were specifically developed for Ge-containing substrates on Si, where GeSn or Ge are the host materials for the QDs and for two types of quantum device architectures prototypic to (i) NW/fin-FET devices and (ii) planar quantum well (QW)-type devices, schematically depicted in Figure 1a and b, respectively. Each of the architectures presents its own distinct challenges for the processing modes developed. For example, the NW devices are truly three-dimensional (3D), using conformal deposition of the gate materials (oxide and TiN, metal) to form a π- or gate-all around gates. Notably, realizing multiple split gate architectures (Figure 1f) would not only double the total number of QDs but also provide unique quantization of the QDs at the corners of the NW channel.[5] For the QW-type devices utilizing planar heterostructure substrates (Figure 1b), the patterning challenges are in realizing large densities and varying complexities at ultimately small dimensions of the gates. Although similar architectures have been demonstrated by using EBL in a positive resist and a subsequent metal lift-off, we demonstrate that the HSQ gate definition process brings all of the advantages of extreme resolution and fidelity of patterning. Additionally, we estimated the resistivity of single-line TiN structures with varying line widths and lengths to acquire initial electrical data of the TiN structures obtained.

2. MATERIALS AND METHODS

2.1. Fabrication Modes. The processing steps for the realization of multigate TiN structures are schematically shown in Figure 1g and h for TMAH and salty NaOH development processes, respectively. Note that the processing steps are different due to the need to introduce a sacrificial SiN_x layer on top of the TiN for the salty NaOH HSQ process that, as we show below, is advantageous in achieving the desired small dimensions and high fidelities of the structures. The use of the salty NaOH developer directly on the TiN surface was not successful due to HSQ lifting-off at all of the applied exposure doses. We postulate that this is linked to the use of the NaOH developer (a highly concentrated strong base), which can oxidize and dissolve the surface titanium oxide and cause HSQ lift-off. Substrates used were pure Si and Si substrates with epi-grown GeSn/Ge (480 nm thickness) and GeSi/GeQW/GeSi (about 3 μm thickness) layers. Previously, similar substrates were used to fabricate devices showing record mobilities with NW-FET[21] or 2D hole gas QW devices.[22] Before exposure, substrates were covered by ALD with oxide (either 6 nm HfO or 20 nm AlO_x) and with 50−60 nm ALD TiN. The TiN films were deposited using a plasma-enhanced ALD process with a TDMA[Ti] precursor (heated to 90 °C) in an ALD chamber (Cambridge Nanotech Fiji system) at constant pressure (300 mTorr) and temperature (250 °C). Further details for the ALD process can be

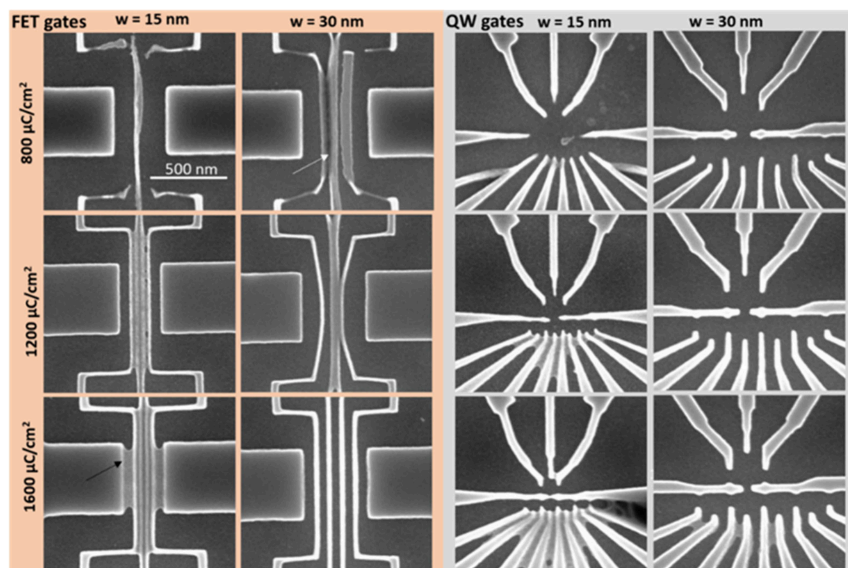

Figure 2. SEM images of HSQ dose tests at varying dose ($\mu C/cm^2$), developed by using TMAH developer for multigate FET (left, beige) and QW (right, gray) architectures. The designs shown are for widths (W) = 15 and 30 nm and spacing ($S = 2W$) exposed on Si, correspondingly.

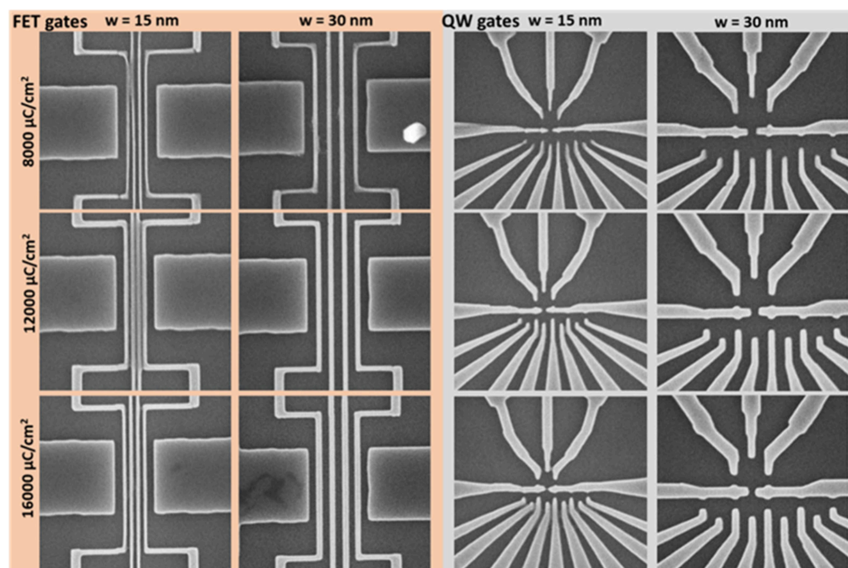

Figure 3. SEM images of HSQ dose tests at varying dose ($\mu C/cm^2$), developed by using a salty NaOH developer for multigate FET (left, beige) and QW (right, gray) architectures. The designs shown are for widths (W) = 15 and 30 nm and spacing ($S = 2W$) exposed on Si, correspondingly.

found elsewhere.[23] For the substrates that were processed with the salty NaOH developer, a 35 nm PECVD SiN_x was deposited on top of the TiN. The EBL exposures were done with two types of gate designs for gate-defined spin-qubit devices as described in Figure 1a and b. Figure S1 in the Supporting Information shows example SEM images of the various gate designs investigated, which can be used for the realization of different number and topology of the QD part of the spin-qubit devices. All images from Figure S1 are for patterns developed on epi-grown Ge-containing layers on Si. Notably, the NW/fin-FET devices use sub-500 nm Ge-containing substrates, while the planar QW-type devices use about 3 μm Ge epi-grown layers. All the patterns examined were exposed by using an Elionix 100 kV EBL system and 3 w/w % HSQ resist that was spin coated at 2000 rpm for 30 s and baked at 120 °C for 3 min to give a 40 nm thick HSQ resist layer. The HSQ resist solution was freshly prepared using HSQ powder dissolved in dry methyl isobutyl ketone (MIBK) solvent, stored at 5 °C, and used within a week from its preparation for exposures. The exposures were done as dose tests starting at the minimal dose possible (determined by the resolution of the pattern generator and a beam step size of 0.5 nm) at a set current; that is, when a 1 nA e-beam current was used, the minimal dose calculated was 4K $\mu C/cm^2$. Various dose test architectures were designed: (i) gate designs for qubit devices seen in Figures 2 and 3 and Figures S1, S2, and S3, (ii) designs for testing TiN etching with width (W) and spacing (S) that were varied starting at W = 10 nm and increasing by 5 nm up to W = 30 nm, and S at $2W$, $3W$, and $4W$ seen in Figure 4 and Figure S4, and (iii) four-probe resistor structures having a single TiN line with different widths starting at 30 nm, seen in Figure 5 and Figure S5. The pattern transfer into the underlying substrates was done by Cl_2-based RIE or consecutive sulfur hexafluoride (SF_6) and Cl_2-based RIE steps. The HSQ resist removal that allows for contacting the TiN multigate structures was done by diluted buffered oxide etch (BOE) for 30 s, while the HSQ/SiN_x was removed by a combination of BOE and a SF_6/O_2 dry etch process. The final step was Ti/Au (100 nm) metal evaporation and lift-off in defined pads/lines to form metal contact pads for electrical testing.

2.2. Structural Inspection and Electrical Testing. After every processing step, the substrates were imaged to obtain high-resolution

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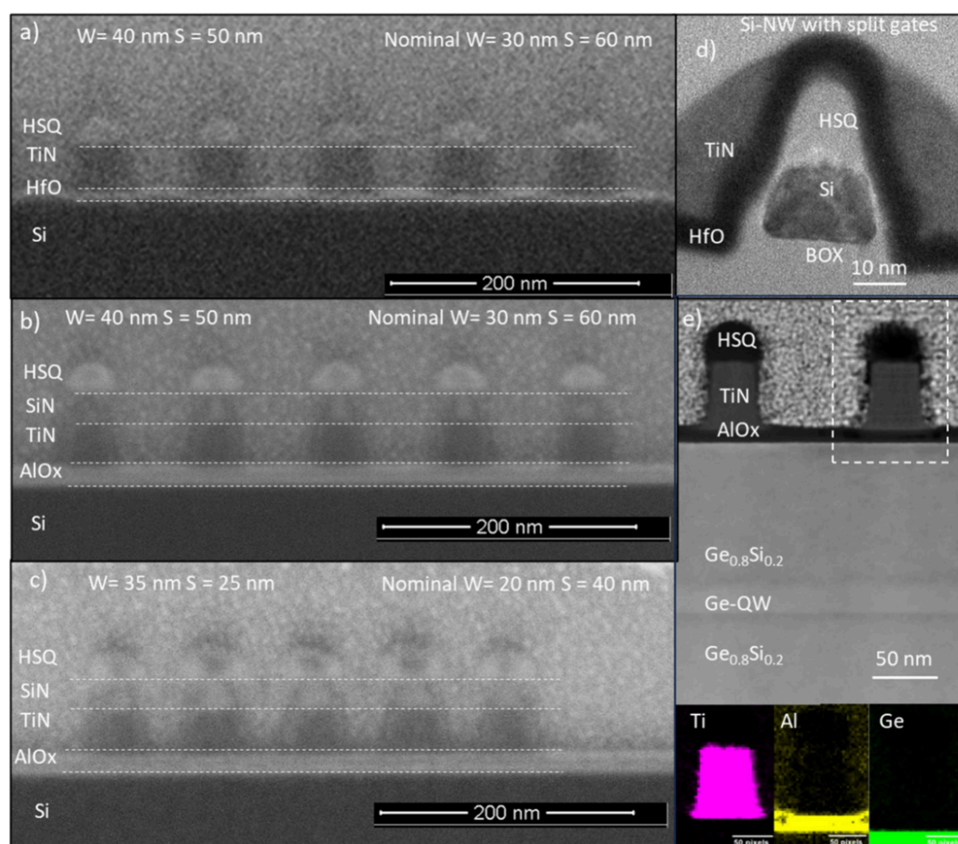

Figure 4. Selection of cross-sectional images demonstrating the high fidelity of the TiN RIE pattern transfer processes developed. a) SEM image of an array patterned using HSQ TMAH developer and etched using Cl_2-RIE with HfO as an etch stop. b and c) SEM images of arrays patterned using salty NaOH developer and consecutive application of SF_6 (SiN_x RIE) and Cl_2-RIE with AlO_x as an etch stop. Insets depict measured and nominal dimensions of the arrays; note the difference in the density of the arrays. d) STEM image of a split-gate TiN/HfO FET device on SOI and e) STEM image of TiN/AlO_x gates on a $Ge_{0.8}Si_{0.2}$/GeQW/$Ge_{0.8}Si_{0.2}$/Si substrate with corresponding EDX elemental mapping taken for one of the gates.

top-down SEM images on a Helios Nanolab dual-beam SEM/FIB instrument using a 5 kV acceleration voltage and through-lens detector. The instrument was also used to obtain cross-sectional SEM images of the patterned structures as well as energy dispersive X-ray (EDX) analysis with an Oxford Instrument X-Max 100 detector. Additionally, selected samples were sectioned by using the instrument to obtain thin lamella samples for cross-sectional STEM imaging. The site-selective sample preparation followed well-established protocols with the final thinning of the foil at low Ga-ion beam energies. The lamella prepared were imaged using JEOL 2100 TEM and Titan STEM instruments equipped with EDX detectors for elemental mapping. To determine the resistivity of a material, a four-point contact measurement was conducted. Four source measure units (SMUs) were used, with connections made at designated points on the sample (see the Supporting Information for further information on the electrical testing setup used).

3. RESULTS AND DISCUSSION

3.1. HSQ EBL Patterning. The first step in the TiN gate definition process, schematically described in Figure 1g and h, is the HSQ EBL patterning. Briefly, a lower dose, e.g., 800 μC/cm^2, results in underexposed features falling over on their side walls (marked in the figure with white arrows), while at larger dose, the structures are not well resolved due to overexposure (indicated in the figure with black arrows). These effects are seen across both FET- and QW-type architectures. Hence, the processing window for patterning gate structures with a 15 nm width (W) and spacing between neighboring lines $S = 2W$ is very limited. In contrast, well-developed structures with W = 30 nm are seen for both architectures, with the QW-type patterns requiring lower exposure dose due to the higher number of line structures and more complex architecture. In all cases, due to proximity effects (the presence of structures in proximity), the actual dose per line is enlarged, which results in larger measured widths of the structures than the nominal and reduced S, correspondingly. To address the need for higher density (smaller W and S) gate structures, we have studied patterning using a salty NaOH developer. The use of the salty NaOH developer required sacrificial SiN_x, acting as an additional hard mask to be introduced as explained in the Materials and Methods section. Figure 3 summarizes the dose test results, showing that the smaller width (W = 15 nm) structures from both NW-type and QW-type designs, which are inaccessible by the TMAH developer, can be successfully patterned. There is a clear enhancement in the resolution and fidelity of the HSQ patterning, allowing high-density gate arrays to be developed. This agrees well with the substantially improved resolution and fidelity of HSQ patterning ever since the salty NaOH developer was introduced[24] and is further confirmation that its use does not preclude its application in CMOS manufacturing.[25]

Extending further the HSQ EBL process to epi-grown Ge-containing layers on Si (which are of interest for quantum devices as elaborated above) has some limitations, as demonstrated by us before.[19] In our previous report, we

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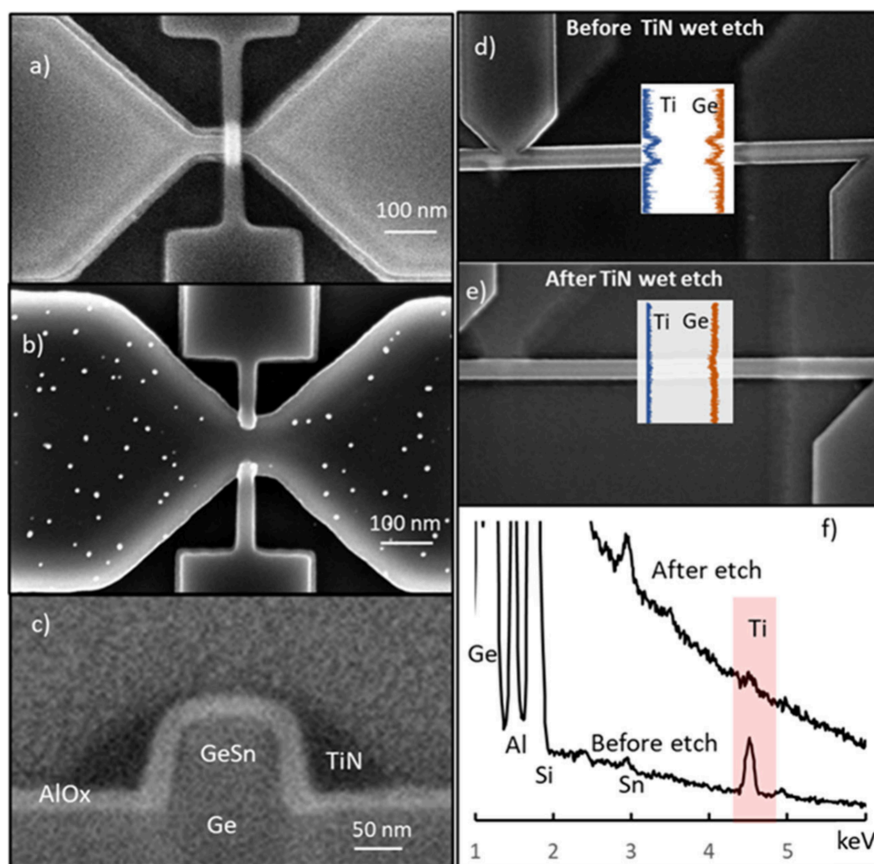

Figure 5. Top-down SEM images of the two main FET gate architectures developed by the TiN gate definition process. a) Single π-gate and b) double split-gate FET based on GeSn/Ge fin channel and conformal ALD AlO_x/TiN gate stack. c) Corresponding cross-sectional SEM image in the area outside the gate depicting TiN residuals. Test GeSn/Ge fin structures after AlO_x/TiN ALD and TiN Cl_2-RIE d) before and e) after APM treatment (insets show corresponding EDX line scans across the fins) and f) accompanying EDX sum spectra showing disappearance of the Ti-signal after APM treatment. Note the appearance of the signals for Ge, Al, Si, and Sn as expected.

showed that Ge produces a larger number of back scattered electrons (BSEs) in comparison to Si, with the highest BSE emission coming from about 5 μm from the top surface. This is the main reason for the increased proximity effect (over-exposure and increase in width of the structures in an array). This effect at 100 kV is not specific to the top TiN/oxide sacrificial layers when they are in the nanometer range but to the underlying substrate. The effect can be minimized by reducing the thickness of the Ge epi-grown layers, hence the contribution of the BSE emission. Here we confirm that by introducing the gate stack (TiN/AlO_x) on the epi-Ge/Si substrates, the HSQ EBL exposures follow a similar trend. The dose test exposures for the TiN/AlOx/Ge/GeSn/Ge/Si substrates with overall thickness of the Ge layers of 480 nm show that the optimal dose range and fidelity of the structures are close to those for the Si exposures (Figures 2 and 3) for both TMAH and salty NaOH developers, correspondingly (Supporting Information, Figures S2 and S3). This is not the case when the Ge-epi layers are over a few microns thick (data not shown) with largely overexposed features observed. Most importantly, Figures S2 and S3 once more demonstrate that the salty NaOH development is superior in achieving overall nominally small dimensions and high fidelity. Specifically, for the QW-type devices where higher complexity and density of the gates are required, and the unwanted proximity effects due to the thicker Ge-containing epi-layers are unavoidable, the HSQ salty NaOH development process offers resolution down to <30 nm gate widths at largely improved side wall roughness in comparison to the other EBL patterning techniques using lift-off. Additionally, to the best of our knowledge, Figure S3 demonstrates the smallest, reported to date, W (15 nm) and S (30 nm) array structures, developed on GeSn/Ge-containing substrates.

3.2. Pattern Transfer in TiN by Reactive Ion Etching. The next step in the TiN gate fabrication sequence is the pattern transfer into the underlying TiN layer. This is done by a Cl_2-based RIE process for substrates where the HSQ structures are formed directly on the TiN (process sequence from Figure 1h). The exposures were done on TiN/HfO or TiN/AlOx sacrificial layers on Si by using a test architecture comprising an array of five lines with varying widths and spacing, starting nominally at $W = 10$ nm and $S = 2W$, $3W$, and $4W$. Examples of the etched samples are shown as cross sections in Figure 4, and corresponding top-down images can be seen in Figure S4 in the Supporting Information. The cross-sectional SEM image of the TiN array patterned by the TMAH developer process using 6 nm of hafnium oxide (HfO) as the gate dielectric and an etch stop is shown in Figure 4a. Note that both the gate metal (TiN) and gate dielectric (HfO) are developed by ALD in the same chamber and that the actual widths of the lines are larger due to a proximity effect during patterning. Figures 4b and c depict TiN arrays developed by the salty developed process etched by a consecutive application of SF_6-based (SiN_x etch) and Cl_2-based (TiN) RIE recipes for

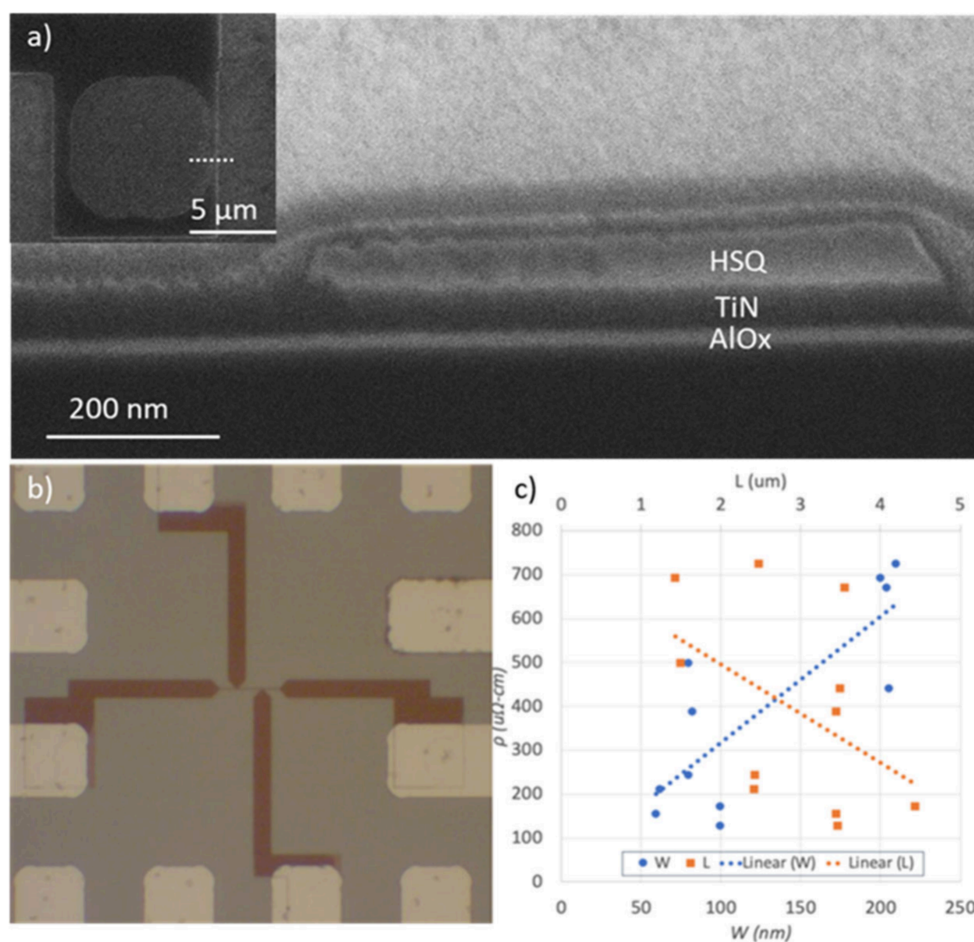

Figure 6. a) Cross-sectional SEM image taken in the contact pad area (inset in part a). b) Optical microscopy image of a fully fabricated four-terminal single-line TiN resistor device fabricated following the processing sequence outlined in Figure 1g. c) Scatter plot resistivity data for TiN single lines with varying width and length measured in a four-probe configuration.

substrates with a sacrificial SiN_x mask (patterning sequence from Figure 1g). The images show slightly overetched SiN_x structures, adopting typical mushroom-type morphologies, which are further transferred with good fidelity into the underlying TiN using 20 nm AlO_x as an etch stop. In all cases we obtained well-defined TiN arrays, with varying density arrays with good clearance between neighboring TiN lines. We note that denser and smaller width arrays, with sub-20 nm width (Figure SI4 c), showed difficulties in full etch clearance of the TiN down to the underlying oxide. Although the array appeared with well-resolved topology by top-down SEM imaging, residual HSQ resist between neighboring lines and connected TiN lines were observed by cross-sectional imaging. This effect has already been described by us, demonstrating an important metrology parameter for well-developed arrays by using HSQ EBL and subsequent etching.[19] Notably, the line-to-line etch clearance effect is not observed in single-line exposures (Figure S4d), where the highest resolution TiN line width structure, reported here at 10 nm, can be seen.

In the following paragraphs we show examples of device topologies developed for the HSQ EBL and TiN etching steps, which were further processed to operational devices by using mix and match EBL and optical lithography, and relevant metallization. Such devices are currently being investigated at cryogenic temperatures for their performance as gate-defined quantum dot architectures (NW/fin or QW types) for spin-based qubits. Figure 4d shows a cross-sectional STEM image from a Si-NW FET device developed on a silicon on insulator (SOI) substrate, where the TiN gates are formed as double split gates (schematics from Figure 1f). The image clearly shows all the nanoscale components of a split gate FET device with the Si channel, HfO gate dielectric conformally covering the channel at its sides, and the TiN split gates that can be used to form QDs at the side walls or corners of the channel. Following similar process steps, we also patterned fin-type architectures on GeSn/Ge substrates with single π- and doubled split-gates (Figure 5a and b). Additionally, Figure 4e demonstrates the applicability of the HSQ TiN gate definition process to planar substrates such as $Ge_{0.8}Si_{0.2}$/GeQW/$Ge_{0.8}Si_{0.2}$/Si that were used previously to form high-mobility two-dimensional Ge-hole gas devices.[22] Specifically, the STEM image in Figure 4e shows two gates from an array of gates, as shown in the top-down SEM image from Figure S1d, whereby the Ti, Al, and Ge EDX spectral mapping validates the high fidelity and the excellent clearance of the TiN lines following the etching process.

The Si NW-type FET (Figure 4d) or the GeSn fin-type FET (Figure 5a and b) architectures require initial NW or fin definition, followed by conformal gate stack formation and TiN RIE etching to define the gates. Due to the nonplanar topology provided by the side wall facets of the NW/fin channel and the inherent high directionality of the RIE

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process, small TiN spacers (small side-wall residuals) can be formed, as evidenced by the cross-sectional SEM image in Figure 5c. The existence of such residuals will be detrimental to the performance of the multigate NW/fin FET devices as the gates will be electrically connected via the side-wall TiN spacers running parallel to the direction of the channel. To alleviate this, we developed an additional wet chemical TiN isotropic etch recipe that we refer to as a TiN cleaning step. A similar approach has been used when investigating the wet etching of TiN in confined nanospaces.[26] Briefly, the wet etch chemistry for this process is based on using a conventional ammonia−peroxide mixture (APM) that is capable of nanometric removal of TiN by surface oxidation of the TiN to TiO_2 and its dissolution under dilute ammonia. The completion of the etch was followed by EDX elemental line scans as depicted in Figure 5d−f. The TiN residuals were fully removed after 8 min of APM treatment, determined by the disappearance of the Ti signal in the EDX line scans, with the corresponding EDX spectrum plots shown in Figure 5f. Please note that the AlO_x layer is not affected by the TiN cleaning step, as seen by the appearance of the Al signal in the EDX and additional cross-sectional images (data not shown).

3.3. Resist Removal for Metallization and Electrical Testing. In order to develop metal contacts to the TiN gate structures, the EBL mask (HSQ or HSQ/SiN_x) removal needs to be implemented, as schematically shown in Figure 1h and g. That is done after the optical lithography for contact pads' definition. It is followed by dilute BOE etching (HSQ removal), and it is further succeeded by a SF_6-based RIE when the process sequence started with a HSQ/SiN_x mask. Figure 6a shows a cross-sectional SEM image of a contact pad after the BOE treatment and before metallization. It confirms that the HSQ is fully removed and that the overall TiN thickness was not substantially reduced after the treatment. AFM was used to evaluate changes in the surface morphology in the TiN contact pad area after the HSQ removal step. The data show that while the HSQ mask can be successfully removed, the surface roughness of the underlying TiN is increased. Figure 6b depicts an example of a fully fabricated four-terminal TiN resistor device having about a 100 nm TiN contact line. Using such four-terminal, single-line resistor devices with varying width and length, we obtained initial TiN resistivity data summarized in Figure 6c. The scatter plot shows that the resistivity values are in the range of about 150−700 $\mu\Omega$-cm and agree well with the results of other published results for ALD-deposited TiN films, including the sheet resistance data from the ALD process optimization runs done at our clean room facilities.[23,27] In all cases, ohmic I/V curves were obtained (Figure S4b). For the range of diameters examined, the resistor data suggest no dependence on the TiN line width. Future electrical performance measurements including low temperature (down to the mK regime) are planned to elucidate the performance of the TiN lines developed by the process modes described above as multigates for qubit devices.

4. CONCLUSIONS

In this paper we formulate and systematically study the processing sequences for forming TiN multigate arrays with high resolution (down to 15 nm in width), density, and fidelity. The processing modes based on EBL patterning were applied to define multigate architectures that can be part of NW/fin FET and QW-type devices. Such devices can be used for realizing gate-defined QDs and further demonstrate spin-based qubits hosted in GeSn and Ge-QW. From a materials processing perspective, the gate definition processes described here are alternatives to the commonly used metal lift-off gate definition, intended to allow for architectures with high complexity and applicability to various device concepts but also to provide high fidelity and resolution during patterning.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.4c01499.

Additional top-down SEM images of the HSQ exposures at optimal dose for various multigate architectures and complexities, as well as at exposures at varying dose developed by using TMAH and salty NaOH developers on TiN/AlOx/GeSn/Ge on Si substrates; four contact electrical testing setup and I/V plots of single TiN resistor devices developed using the TiN processing modes studied (PDF)

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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