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Electrical characterization of n-doped SiGeSn diodes with high Sn content

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Abstract
Diodes incorporating undoped and Sb-doped Si1−x−yGe1−x−ySnx layers grown by molecular beam epitaxy with different alloy compositions and lattice-matched to Ge were fabricated and characterized experimentally. We discuss material as well as electrical device characterization and investigate different contact metallizations (Ni and Al). In particular, we investigate the formation of Ni(Si1−x−yGe1−x−ySnx) on the doped Sb-doped Si1−x−yGe1−x−ySnx layers via annealing based on material characterization and measurements of specific contact resistivities. Our results can serve as a starting point for the investigation of Si1−x−yGe1−x−ySnx layers with high Si and Sn content as cladding material in optoelectronic devices such as lasers and light emitting diodes.

Keywords: SiGeSn, Sb doping SiGeSn, Ni(SiGeSn), annealing, Ni, Sn

(Some figures may appear in colour only in the online journal)

1. Introduction
In the past few years, the interest in a group IV light emitting device that can be easily integrated with Si photonics and electronics has increased. While the binary Ge1−ySnx has been shown to be a direct bandgap material for large enough Sn content, the ternary alloy Si1−x−yGe1−x−ySnx could also be a direct bandgap material in a certain compositional range with a lattice constant that can be adjusted more easily [1]. Si1−x−yGe1−x−ySnx has been proposed as barrier material in Ge1−ySnx/Si1−x−yGe1−x−ySnx multi-quantum well structures [1] and has successfully been incorporated experimentally into Si1−x−yGe1−x−ySnx and Ge1−ySnx/Si1−x−yGe1−x−ySnx multi-quantum well diodes [2, 3]. Furthermore, doped Si1−x−yGe1−x−ySnx can serve as cladding material for active Ge1−ySnx layers with lower bandgaps in optoelectronic devices such as light emitting diodes or lasers. Challenges in layer growth of the ternary alloys include accessing alloy compositions with high Si and Sn content as well as the doping of Si1−x−yGe1−x−ySnx structures for electro-optical device applications. While the growth of undoped bulk Si1−x−yGe1−x−ySnx has successfully been achieved for alloys with x = 0.41 and y = 0.11 [4], molecular beam epitaxy (MBE) can be used to grow ternary alloys with even higher Si (and Sn) content [5, 6], thus extending the accessible compositional range for the ternary alloy. Both n- and p-type doping in CVD-grown Si1−x−yGe1−x−ySnx layers as well as their incorporation into Ge/Si1−x−yGe1−x−ySnx heterojunction diodes has been shown [7–11], however, those studies were restricted to alloy compositions with high Ge content (1−x−y ≥ 0.75).

Finally, the incorporation of doped Si1−x−yGe1−x−ySnx into optoelectronic devices requires contacts with low specific contact resistivities to minimize ohmic losses. As with the binary alloys Si1−x−yGe1−x−ySnx, the deposition of Ni onto Si1−x−yGe1−x−ySnx, followed by annealing for silicongermanidation has been shown to lead to the formation of NiSi1−x−yGe1−x−ySnx with potentially low specific contact resistivities [12], however, alloys with Ge content <0.79 have not yet been investigated.

In this work, we present results on the characterization of Si1−x−yGe1−x−ySnx pin diodes with different alloy compositions and a Sb-doped Si1−x−yGe1−x−ySnx top contact layer. We show details on the material characterization of the Si1−x−yGe1−x−ySnx...
layers as well as on fabrication and electrical characterization of the devices. In particular, we compare Al and Ni/Al contact metallizations with respect to their specific contact resistivities and investigate the formation of Ni(Si$_x$Ge$_{1-x}$)$_{2}$ via annealing as well as the influence of the annealing process on specific contact resistivities.

2. Fabrication and processing

All semiconductor layers were grown using solid-source MBE on 4° B-doped Si (100) substrates with a nominal resistivity of $\rho = 0.01$ $\Omega$cm. Layer growth started with an initial 50 nm Si layer at substrate temperature $T = 600^\circ$C to smoothen the surface and cover remaining surface contaminants. A pin heterojunction layer structure was used for all devices as shown schematically in figure 1. The p-doped region was formed by a 400 nm thick B-doped Si ($N_A = 10^{20}$ cm$^{-3}$) layer and a 100 nm B-doped Ge ($N_A = 10^{20}$ cm$^{-3}$) layer. The B-doped Ge layer was deposited at a substrate temperature $T = 330^\circ$C. Subsequent annealing starts with a temperature ramp up to a substrate temperature of $\sim$850°C and is held for 300 s to create a virtual substrate (VS).

The high temperature serves to decrease the threading dislocation defects caused by the lattice mismatch between Si and Ge. Afterwards, a 100 nm thick intrinsic Si$_x$Ge$_{1-x}$ Sn$_y$ layer was deposited, followed by an additional Sb-doped Si$_x$Ge$_{1-x}$Sn$_y$ layer (with nominal doping concentration $N_D = 10^{20}$ cm$^{-3}$) to form the n-contact. Three different alloy compositions were selected and chosen to approximately match the lattice constant of the underlying Ge. Material composition and strain were investigated using x-ray diffraction (XRD) and Rutherford backscattering spectroscopy (RBS) [13]. RBS measurement results are reported in table 1. Figure 2 shows the reciprocal space maps around the (-2-24) Bragg reflection for the three alloy compositions. The lattice matching to the underlying Ge- VS can be seen to be almost perfect for samples B, E as the Ge and Si$_x$Ge$_{1-x}$Sn$_y$ peaks coincide. For all other samples two overlapping peaks are visible, indicating that the Si$_x$Ge$_{1-x}$Sn$_y$ layers are pseudomorphic on Ge and that lattice matching is good, i.e. strain in the Si$_x$Ge$_{1-x}$Sn$_y$ layers is negligible. In order to investigate the dopant distribution in the Sb-doped Si$_x$Ge$_{1-x}$Sn$_y$ layer, secondary-ion mass spectroscopy was performed (figure 2(b)). The results show that the Sb doping profile is homogeneous for the first $\sim$85 nm in the n-doped Si$_x$Ge$_{1-x}$Sn$_y$ layer and that the dopant concentration is comparable in all samples.

The MBE layers were processed into single mesa diodes. A SiO$_2$ hardmask defined by optical lithography with AZ

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**Figure 1.** Schematic cross section of (a) the MBE layer structure and (b) the fabricated devices.

**Figure 2.** (a) RSM around the (-2-24) Bragg reflection for the three alloy compositions, see table 1 and (b) SIMS of nominal Sb concentration profile in the three alloys.

**Table 1.** Si$_x$Ge$_{1-x}$Sn$_y$ alloy compositions extracted from RBS [13].

<table>
<thead>
<tr>
<th>Samples</th>
<th>Si (%)</th>
<th>Ge (%)</th>
<th>Sn (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, D</td>
<td>26.5</td>
<td>66.0</td>
<td>7.5</td>
</tr>
<tr>
<td>B, E</td>
<td>37.5</td>
<td>53.0</td>
<td>9.5</td>
</tr>
<tr>
<td>C, F</td>
<td>46.1</td>
<td>41.5</td>
<td>12.4</td>
</tr>
</tbody>
</table>
5214 resist and reactive ion etching was used to pattern the surface with circular mesas. An inductively coupled plasma (ICP) dry etching step using Cl₂/HBr was used to structure the mesa with heights between 358 and 406 nm. The devices were cleaned from photoresist by O₂ plasma, the oxide was removed with a 60 s BHF dip. Additional cleaning steps were used to prepare the surface for the deposition of the passivation layer. A 260 nm thick SiO₂ layer was deposited at a substrate temperature \( T = 250 \, ^\circ\text{C} \) by plasma enhanced chemical vapor deposition (PECVD) to passivate the semiconductor surface. A second optical lithography step with AZ 5214 resist followed by a dry etching step with CHF₃ plasma was used to define and open contact windows. To investigate the difference in contact metallization two materials were chosen, see table 2.

On one half of the samples (samples A–C) 1.4 \( \mu \text{m} \) Al was sputtered to form the metal contact. Optical lithography, ICP dry etching and a \( \text{H}_3\text{PO}_4 \) wet etching step to remove any additional metal were used to structure the metal contacts. The contact pads of the other half of the samples (samples D–F) were defined through optical lithography. A HF dip was used to clean the surface prior to the deposition of 30 nm Ni and 470 nm Al by e-beam evaporation followed by a lift-off step. A schematic cross section of the fabricated pin diodes is shown in figure 1(b). The radii of the circular mesas vary between 1.5 and 80 \( \mu \text{m} \). Figure 3(a) shows a scanning electron microscope (SEM) image of a tilted diode with a mesa radius of \( r = 80 \, \mu\text{m} \). The top metal contact pad and the surrounding bottom metal pad are visible. A cross section of the same diode is shown in figure 3(b). The different MBE layers are clearly visible. In the SEM image the difference between the Ge and the \( \text{Si}_x\text{Ge}_{1-x-y}\text{Sn}_y \) layer can be observed.

### Table 2. Overview of the samples with two contact metallization.

<table>
<thead>
<tr>
<th>Samples</th>
<th>Contact metal</th>
<th>Special treatment</th>
</tr>
</thead>
<tbody>
<tr>
<td>A, B, C</td>
<td>1.4 ( \mu \text{m} ) Al</td>
<td>None</td>
</tr>
<tr>
<td>D, E, F</td>
<td>30/470 nm Ni/Al</td>
<td>None</td>
</tr>
</tbody>
</table>

3. Results and discussion

3.1. Electrical characterization

The devices were characterized electrically using a Keithley 4200 semiconductor analyzer. The current density–voltage characteristics (J–V curves) for representative diodes with identical diameters are shown in figure 4 for samples D–F with Ni/Al contacts (figure 4(a)) and for samples A–C with Al contacts (figure 4(b)). All samples show diode behavior, indicating that the MBE-based doping by Sb co-evaporation to obtain n-doped \( \text{Si}_x\text{Ge}_{1-x-y}\text{Sn}_y \) layers was successful. Comparing the averaged current density at \(-0.8 \, \text{V} \) (figure 5) for all measured devices it can be seen that the dark current density is lowest for samples B and E with a Sn content of \(~9.5\%\). This could be a result of the fact that the lattice matching conditions for the \( \text{Si}_x\text{Ge}_{1-x-y}\text{Sn}_y \) layer to the underlying Ge
has been met most closely for samples B and E. A transmission line model (TLM) is used to investigate specific contact resistivities of the different metallic contacts. Linear TLM structures were measured and the resulting data was fitted using the expression

\[ R(l) = 2 \cdot R_C + \frac{R_{sh}}{L} \cdot l. \]  

(1)

Here, \( R_C \) is the contact resistance, \( R_{sh} \) is the semiconductor sheet resistance, \( L \) is the length of the contact (204 \( \mu m \)) and \( l \) is the distance between adjacent contact pads. The specific contact resistivity for each sample can then be obtained using equation (2) with the values for \( R_C \), \( R_{sh} \) obtained from data fitting and the contact length \( L = 204 \mu m \) (with transfer length \( L_C \)):

\[ \rho_C = \frac{(R_C \cdot L)^2}{R_{sh}} = L_C^2 \cdot R_{sh}. \]  

(2)

Figure 6 shows the dependence of the specific contact resistivity on the Sn content in the Si\(_x\)Ge\(_{1-x}\)Sn\(_y\) layers for the different metallic contacts. The Al metal contacts exhibit an average specific resistivity of \( 4.5 \times 10^{-5} \text{ Ohm cm}^2 \) (7.5% Sn) and \( 3.0 \times 10^{-5} \text{ Ohm cm}^2 \) (9.5% Sn). For the Ni/Al contact an average specific contact resistivity of \( 3.3 \times 10^{-6} \text{ Ohm cm}^2 \) (7.5% Sn) and \( 2.3 \times 10^{-6} \text{ Ohm cm}^2 \) (9.5% Sn) could be extracted. These values are consistently lower than for the Al contacts. For 12.4% Sn the difference between the two contact materials is negligible according to the extracted specific contact resistivities.

3.2. Annealing investigations

While Ni/Al contacts clearly show lower specific contact resistivities than the Al contacts, we expect the contacts to improve further upon annealing. Previous investigations have shown that the deposition of Ni onto Si\(_x\)Ge\(_{1-x}\)Sn\(_y\) followed by annealing leads to the formation of Ni(Si\(_x\)Ge\(_{1-x}\)Sn\(_y\)) with potentially low specific contact resistivities [12]. Here, we subjected all samples with Ni/Al contacts to annealing steps in order to investigate the influence on specific contact resistivities.
Samples D–F (see table 2) with 30 nm Ni and 470 nm Al were annealed for 30 s in N₂ at two different substrate temperatures (300 °C and 325 °C). The impact of the annealing steps was investigated quantitatively again based on TLM results. Qualitatively, however, the annealing step can be seen to lead to the formation of a phase containing Ni in the top Si₁₋ₓGeₓSnₓ layer in cross sectional SEM images of the diodes after annealing: an additional layer with a thickness of approximately 70 nm can be observed after annealing with T = 325 °C and t = 30 s (figure 7(a)) compared to figure 3(b). We confirm the existence of a phase containing Ni in the top Si₁₋ₓGeₓSnₓ layer with XRD measurements that will be discussed in the following subsection.

Figure 7(b) shows the specific contact resistivity as a function of temperature for various Sn contents. Surprisingly, the specific contact resistivity can be seen to increase with increasing annealing temperature. As shown in figure 2(b) the Sb doping concentration in the n-doped Si₁₋ₓGeₓSnₓ layer is homogeneous with a layer thickness of ~85 nm. This thickness, however, is comparable to the thickness of the Ni-rich contact layer within the n-doped Si₁₋ₓGeₓSnₓ (~70 nm). As a result, we cannot discount the possibility that the Ni-rich contact layer effectively contacts the intrinsic Si₁₋ₓGeₓSnₓ layer, which could explain an increased specific contact resistivity. Using a thicker Sb doped Si₁₋ₓGeₓSnₓ layer (~200 nm) in future sample growth could solve this issue.

Another explanation for the increase in specific contact resistivity with increasing annealing temperature could be the formation of Ni₅(Si₁₋ₓGeₓSnₓ)₃ rather than Ni(Si₁₋ₓGeₓSnₓ) during annealing and a resulting increase in specific contact resistivity. Therefore, we also performed an XRD analysis, which will be discussed in the next subsection.

3.3. Ni₅(Si₁₋ₓGeₓSnₓ) alloy formation

Additional experiments were performed in order to investigate the Ni₅(Si₁₋ₓGeₓSnₓ) contact formation in our layers. To carry out these experiments, additional samples were fabricated based on Si₁₋ₓGeₓSnₓ with the three different concentrations reported in table 1. Here, the samples were covered with unstructured Ni layers with a thickness of 30 nm and then subjected to different annealing steps. The surface morphology was investigated in the SEM and XRD measurements were used to investigate whether Ni₅(Si₁₋ₓGeₓSnₓ)₃ or Ni(Si₁₋ₓGeₓSnₓ) was formed. In figure 8, SEM images show the surfaces of the different samples after annealing steps at T = 300 °C and T = 325 °C in N₂ for 30 s. While no clear surface changes can be observed in the Si₀.2₆₅Ge₀.₆₆Sn₀.₀₇₅ sample as the annealing temperature is increased from T = 300 °C to T = 325 °C, the same increase
can be seen to lead to the formation of droplets on the \( \text{Si}_{0.375}\text{Ge}_{0.53}\text{Sn}_{0.095} \) sample surface for the sample with higher Sn content. The \( \text{Si}_{0.461}\text{Ge}_{0.415}\text{Sn}_{0.124} \) sample with the highest Sn content shows droplets on its surface for both annealing temperatures. Further investigations using energy-dispersive x-ray spectroscopy (EDX) were carried out to determine the material composition of the droplets. Figure 9 presents the results of the EDX analysis for the elements Ge, Si, Sn and Ni on the sample surface of the \( \text{Si}_{0.375}\text{Ge}_{0.53}\text{Sn}_{0.095} \) sample. Ge and Si are distributed nearly homogeneously on the sample surface except for some places, where the signal intensity drops markedly. These positions coincide with positions with high intensity for the Sn material analysis (colored purple) as well as with the positions of the precipitates seen in the SEM inset. Therefore, the droplet formation is as a result of Sn precipitation as Ni is incorporated.

Finally, figure 10 presents the 2 theta scans obtained through XRD to investigate the phase formation of \( \text{Ni}(\text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn}) \) for annealing temperatures \( T = 300 \, ^\circ\text{C} \) and \( T = 325 \, ^\circ\text{C} \). Peaks around \( 45^\circ \) are observed for all samples at all annealing temperatures. We attribute these to the formation of the mono-\( \text{Ni}(\text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn}) \) phase for all samples and annealing temperatures [12]. We also investigated the effect of annealing on the semiconductor layers underneath the \( \text{Ni}(\text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn}) \) contacts by rocking curves (figure 11). While annealing can be seen to reduce the intensity of the \( \text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn} \) peaks, which can be attributed to the fact that the formation of \( \text{Ni}(\text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn}) \) reduces the thickness of the \( \text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn} \) layers by \( \sim 70 \, \text{nm} \), the peak shape remains largely unchanged. Furthermore, we do not observe the formation of additional peaks that could indicate alloy decomposition of the \( \text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn} \) as a result of the annealing. Based on these results we conclude that the effect of annealing on the \( \text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn} \) semiconductor layers below the \( \text{Ni}(\text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn}) \) contacts is negligible, i.e. the Sn precipitation observed in figure 8 originates mainly from the \( \text{Ni}(\text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn}) \) layer and not from the \( \text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn} \) semiconductor layers below. Future analysis based on transmission electron microscopy could be used to investigate the crystal structure and material composition of the \( \text{Ni}(\text{Si}_{1-x}\text{Ge}_{1-x}\text{Sn}) \) layers in more detail.

Figure 9. EDX analysis for the materials Ge, Si, Sn and Ni on the surface of sample \( \text{Si}_{0.375}\text{Ge}_{0.53}\text{Sn}_{0.095} \) with 30 nm Ni after annealing at \( T = 325 \, ^\circ\text{C} \) for 30 s in a \( \text{N}_2 \) ambient. The inset shows a SEM image of this region on the surface.
4. Conclusion

Si$_x$Ge$_{1-x}$Sn$_y$ alloys allow to decouple the bandgap from the lattice constant for possible applications in optoelectronic devices. We demonstrated the fabrication of Si$_x$Ge$_{1-x}$Sn$_y$ heterojunction pin diodes with three different alloy compositions. We successfully developed a strategy to dope Si$_x$Ge$_{1-x}$Sn$_y$ layers with Sb to create an n-doped top contact. Investigations regarding the metallization with Al and Ni/Al as contact material showed that the use of Ni/Al results in a specific contact resistivity of $\sim 2.3 \times 10^{-6}$ Ohm cm$^2$ (Si$_{0.375}$Ge$_{0.53}$Sn$_{0.095}$) and $3.3 \times 10^{-6}$ Ohm cm$^2$ (Si$_{0.265}$Ge$_{0.66}$Sn$_{0.075}$). Those specific contact resistivities were roughly one order of magnitude lower than for devices with Al metal contacts. Annealing investigations were carried out to investigate the formation of Ni(Si$_x$Ge$_{1-x}$Sn$_y$) contact layers. While we observe an increase in specific contact resistivity rather than a decrease for increasing annealing temperatures, we attribute this to the fact that the Ni(Si$_x$Ge$_{1-x}$Sn$_y$) contact layers extend into the intrinsic Si$_x$Ge$_{1-x}$Sn$_y$ layers of our samples. A thicker Sb doped Si$_x$Ge$_{1-x}$Sn$_y$ layer used for contact formation in future experiments could solve this issue.

Furthermore, we investigated the formation of Ni(Si$_x$Ge$_{1-x}$Sn$_y$) through annealing based on EDX analysis and XRD measurements for all samples and found that, depending on the annealing temperature, the formation of Ni(Si$_x$Ge$_{1-x}$Sn$_y$) can lead to Sn precipitation and the formation of Sn droplets on the sample surface especially for samples with high Si and high Sn content. Optimal annealing temperatures for such alloys have to be investigated further in order to determine processing parameters that enable the reliable formation of contacts to n-doped Si$_x$Ge$_{1-x}$Sn$_y$ alloys with low specific contact resistivities. Other investigations [15] showed that the incorporation of for example Al reduces the diffusion of Ni and can stabilize the reactions of Ni–Si and Ni–Ge.

Our results can form the basis for the fabrication of Si$_x$Ge$_{1-x}$Sn$_y$ layers with high Si and Sn content as cladding material for Si$_x$Ge$_{1-x}$Sn$_y$ and Ge$_{1-y}$Sn$_y$ based optoelectronic devices.

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