Semiconductor Science and Technology

PAPER

Electrical properties of n-type 3C-SiC epilayers *in situ* doped with extremely high levels of phosphorus

To cite this article: Gerard Colston and Maksym Myronov 2018 *Semicond. Sci. Technol.* **33** 114007

IOP Publishing Semiconductor Science and Technology
Semicond. Sci. Technol. 33 (2018) 114007 (6pp) https://doi.org/10.1088/1361-6641/aade67

Electrical properties of n-type 3C-SiC epilayers *in situ* doped with extremely high levels of phosphorus

Gerard Colston and Maksym Myronov[1]

Department of Physics, The University of Warwick, Gibbet Hill Road, Coventry, CV4 7AL, United Kingdom

E-mail: G.Colston.1@warwick.ac.uk and M.Myronov@warwick.ac.uk

Received 29 June 2018, revised 20 August 2018
Accepted for publication 3 September 2018
Published 12 October 2018

Abstract

Low temperature heteroepitaxy of cubic silicon carbide (3C-SiC) on silicon substrates is key to the low-cost and mass scale hetergeneous integration of 3C-SiC into the semiconductor market. Low temperature growth also opens up the opportunity to dope 3C-SiC *in situ* during the epitaxial growth with standard Si based n-type and p-type dopants. *In situ* doping offers many advantages over ion implantation, such as complex doping profiles, more abrupt interfaces and minimal crystal damage. In this study, 3C-SiC thin films have been doped with phosphorus to a range of concentrations during epitaxial growth on standard silicon (Si) substrates. Both the material and electrical properties of the films have been investigated. Hall effect measurements and secondary ion mass spectroscopy profiling confirm 100% electrically active n-type dopants up to $2 \times 10^{20}\,\mathrm{cm}^{-3}$. The process offers extreme control over the 3C-SiC electrical properties without relying on post-growth ion implantation and high temperature activation annealing, enabling the formation of more complex 3C-SiC based devices and low resistance contacts.

Keywords: 3C-SiC, n-type, doping, Hall effect, SIMS

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon carbide (SiC) is a wide bandgap compound semiconductor with properties that lie between those of silicon (Si) and diamond. As such, SiC is well suited to various applications including high power electronics, sensing for harsh environments and radiation resistant photodetectors [1, 2]. Silicon carbide can exist in a number of crystalline structures, known as polytypes, of which the hexagonal structured 4H-SiC and 6H-SiC have been commercially available in the form of substrates since the 1990s [3]. One of the main factors that has held SiC based electronics back is the cost and limited size of these wafers. An attractive solution to this is to grow SiC heteroepitaxially on Si wafers. This can be done using the cubic polytype of SiC, 3C-SiC, however typical growth processes are carried out at high temperatures (~1350 °C), making the process expensive, difficult to scale and resulting in bowed wafers, due to the difference in the thermal expansion coefficients and lattice mismatch between 3C-SiC and Si [4].

Low temperature 3C-SiC growth can reduce the thermal stresses in epi wafers as well as significantly decrease growth costs and allow the growth of 3C-SiC within Si based industrial type cold-wall chemical vapour deposition (CVD) reactors. These reactors generally consist of a quartz chamber which is limited to an upper growth temperature of ~1250 °C which makes achieving highly crystalline 3C-SiC a challenge, however, the throughput of these machines and significant reduction of deposition on the chamber walls would allow mass production of low-cost 3C-SiC/Si epi wafers. Over the last 40 years, various attempts have been made to grow 3C-SiC at low temperatures, however often quality is poor [5], and it relies on complicated growth sequences similar to atomic layer deposition [6] or exotic non-wafer scale growth

[1] Author to whom any correspondence should be addressed

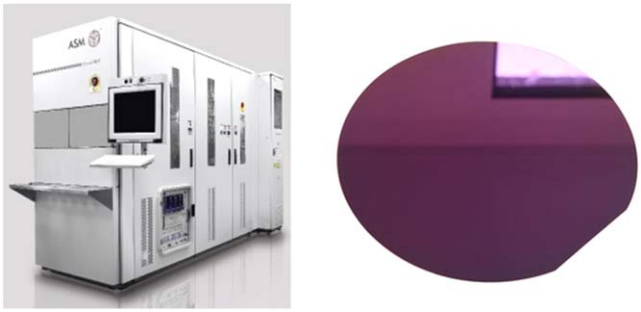

Figure 1. ASM Epsilon 2000 RP-CVD (left), 150 mm diameter 3C-SiC/Si (001) epitaxial wafer (right).

methods such as microwave plasma [7] or hot wire CVD [8]. Recently, high quality 3C-SiC epilayers have been grown using a standard Si based RP-CVD growth system [9]. This process enables the heterogeneous integration of 3C-SiC into the standardised Si platform.

Achieving high levels of electrically active dopants in a 3C-SiC epilayer is crucial for the formation of low resistance Ohmic contacts, controlling material conductivity and forming more intricate structures such as field effect transistors or PiN diodes. Ion implantation is typically employed for SiC polytypes, however, this can be an issue with hetero-epitaxially grown 3C-SiC/Si material as the upper annealing temperature is limited by the melting point of the Si wafer (~1400 °C). Nitrogen (N) is commonly used with SiC as an n-type dopant, however, there are certain drawbacks. Substitutional N has been shown to only occupy the C sites of the SiC lattice, making it less efficient as a dopant. In addition, N has been shown to cause 'kick-out' a process by which a N atom takes a substitutional site but knocks out a C atom from its lattice site leading to an interstitial impurity. This in-turn leads to the formation of inactive complexes which can reduce the electrical activation of the epilayer as a whole [10]. Phosphorus (P), on the other hand, can occupy both the C and Si lattice sites, offering a more effective dopant and is standard within the Si industry. The maximum achievable impurity levels through ion implantation of N or P within 3C-SiC are around $6 \times 10^{20}\,\mathrm{cm}^{-3}$, however, electrical activation at this level of implantation can be around 12%, saturating the free donors at $\sim 7 \times 10^{19}\,\mathrm{cm}^{-3}$ [11] and leaving a high number of interstitial impurities in the crystal.

The aim of this investigation was to demonstrate high levels of P doping in 3C-SiC/Si heterostructures by doping the material during the epitaxial growth process rather than relying on post-growth ion implantation. The as-grown epilayers were characterised using a number of experimental techniques to understand their electrical properties.

2. Experimental details

3C-SiC epilayers were grown on standard on-axis, p^-, 150 mm Si (001) wafers within an ASM Epsilon 2000 reduced pressure chemical vapour deposition (RP-CVD) system at a growth temperature of <1250 °C, see figure 1.

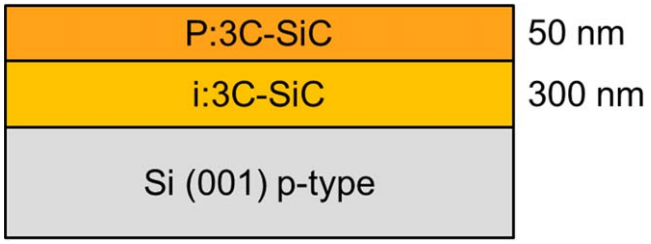

Figure 2. Cross sectional schematic of the P doped 3C-SiC heterostructure.

Table 1. Growth parameters of doped 3C-SiC heterostructures.

Variable	P1	P2	P3	P4	P5
Thickness (nm)	i-300 n-50	i-300 n-50	i-300 n-50	i-300 n-50	i-300 n-50
Relative phosphine flow rate	200	10	1	0.1	0.01

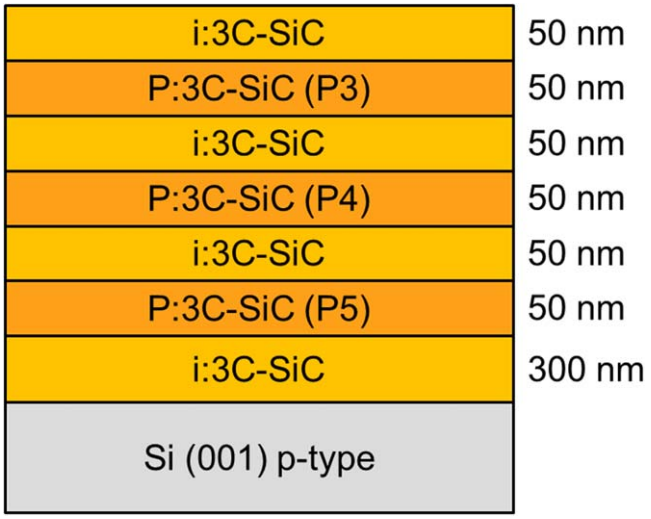

Figure 3. Cross sectional schematic of P doped multilayer heterostructure incorporating doped layers P3, P4 and P5.

Intrinsic 3C-SiC (i:3C-SiC) was grown to a thickness of approximately 300 nm to improve crystallinity and decrease the planar defect density before being capped with a ~50 nm 3C-SiC layer doped with P by the introduction of varying levels of phosphine during epitaxy (P:3C-SiC), see figure 2.

A series of five heterostructures were grown including a range of P doping spanning over five orders of magnitude in the effective dopant flow rate, see table 1.

To investigate the diffusion of P through the 3C-SiC material during growth and assess the profile of the dopants, a multilayer structure consisting of 50 nm thick doped epilayers with 50 nm thick intrinsic spacers between was grown, that incorporated the doping profiles of samples P3, P4 and P5, see figure 3.

The impurity concentration in the five heterostructures was assessed using secondary ion mass spectroscopy (SIMS) profiling carried out by Evans Analytical Group on samples P1, P2 and the multilayer structure. The electrical activity of

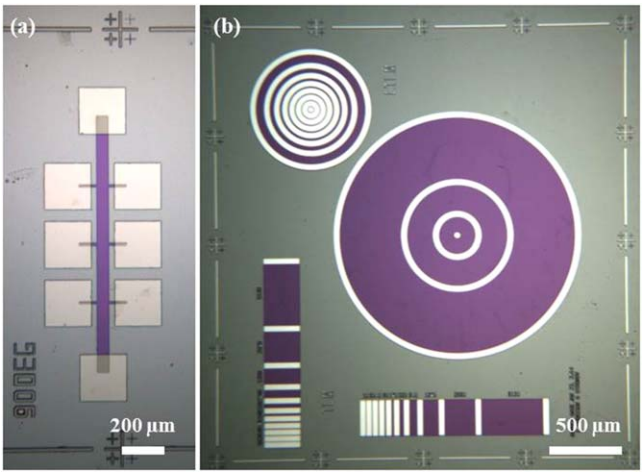

Figure 4. (a) 3C-SiC Hall bar test device structure. (b) 3C-SiC circular and linear TLMs.

the impurities within the 3C-SiC was assessed through Hall effect and resistivity measurements. Hall bars were fabricated through standard photolithography, reactive ion etch dry etching and metal deposition processes, see figure 4. Nickel chromium (NiCr) was deposited as the metal contact for the n-type 3C-SiC by magnetron sputtering. NiCr is an ideal metal contact for n-type 3C-SiC as its work function (∼4.9 eV) is very closely matched to that of doped 3C-SiC, as a non-magnetic alloy it can be sputtered easily and does not readily oxidise. The NiCr contacts of the Hall bars were found to be Ohmic at room temperature so no thermal annealing was needed for Hall bar measurements. The test devices were measured in a variable temperature Hall system over a temperature range of 300–15 K with an AC current of 1 μA passed across the 3C-SiC bar in a magnetic field of ±500 mT. *I–V* sweeps were taken at each temperature for the Hall bar devices to ensure the contacts remained Ohmic over the measurement range.

The contact resistance of the NiCr contacts was further reduced by thermal annealing at temperatures up to 800 °C in an Ar atmosphere within a tube furnace for 10 min. The contact resistance was measured by linear-transmission line measurement (TLM) structures, see figure 4.

3. Results and discussions

3.1. Impurity concentration

The impurity concentrations were extracted by SIMS measurements, the profile of the multilayer structure can be seen in figure 5. High levels of P incorporation up to $5 \times 10^{20}\,\mathrm{cm}^{-3}$ were achieved in sample P1 (not shown here) which utilised the highest dopant flow rate. The SIMS profile of the multilayer shows an ideal linear dependence between the dopant flow rate and the impurity concentration. The interfaces between undoped (i-3C) and doped 3C-SiC can easily be distinguished, however, some spreading on the profile of the P is observed between layers. While the highly

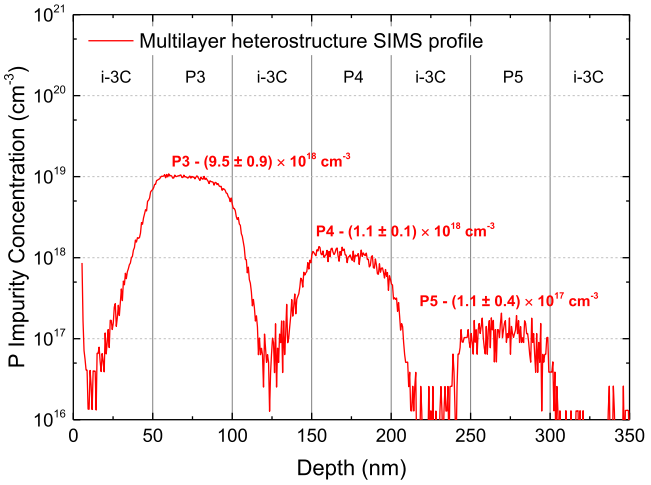

Figure 5. P impurity concentration through the multilayer heterostructure incorporating the doping profiles of samples P3, P4 and P5 as measured by SIMS.

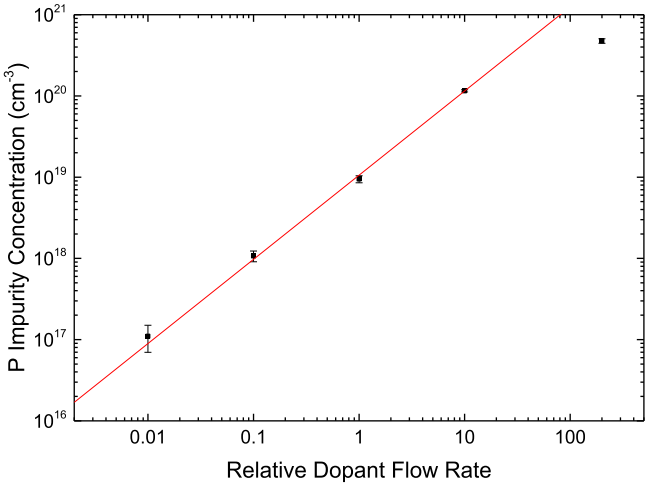

Figure 6. Relationship between impurity concentration and dopant flow rate during the growth of the 3C-SiC heterostructures. Uncertainties on impurity concentration comes from averaging data from the plateaus from each doping region.

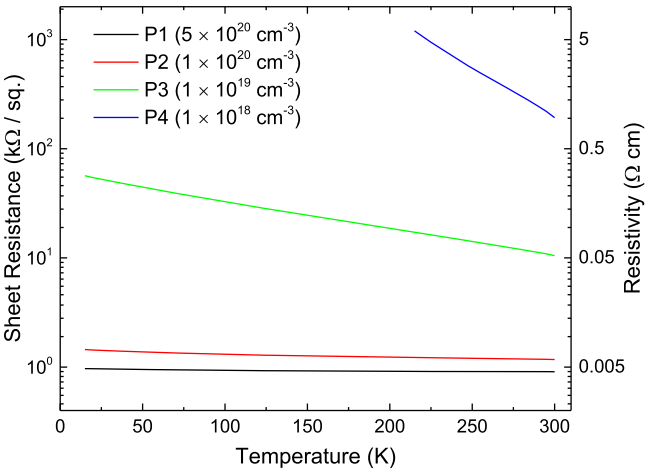

Figure 7. Resistivity of doped 3C-SiC heterostructures. The impurity concentrations shown in the legend are from SIMS measurements.

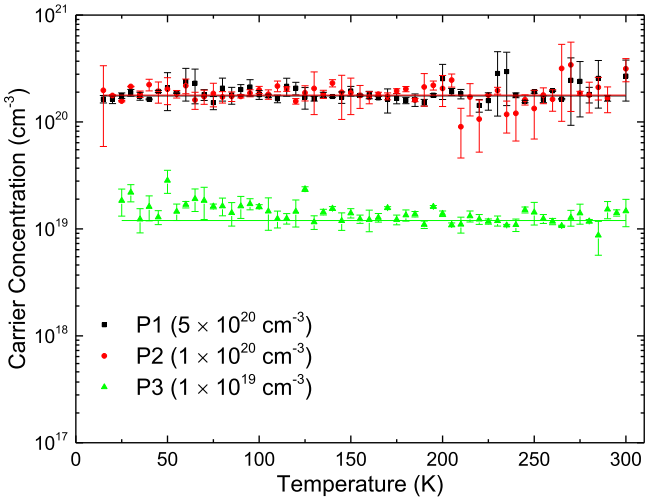

Figure 8. Carrier concentration of the highest doped 3C-SiC heterostructures extracted by Hall effect measurements. The impurity concentrations shown in the legend are from SIMS measurements.

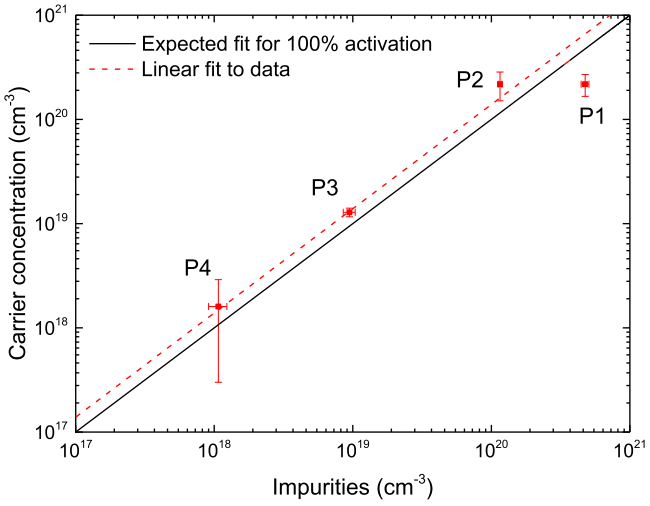

Figure 9. Comparing the impurity concentrations and room temperature carrier concentrations as extracted by SIMS and Hall effect measurements respectively. Uncertainties of carrier concentration are obtained from repeat measurements at room temperature.

energetic SIMS profiling process will cause some spreading of measurements, these results imply the P is diffusing slightly between the layers resulting in non-abrupt interfaces. The distribution at the beginning of the profiles from each doped region appears slightly greater than the tails implying that there may be some P segregation at the surface of the doped epilayers. The impurity concentration decreases at a rate of ~17 nm/decade at the tail of the profile for region P3.

Auto doping of the 3C-SiC with P in the chamber is unlikely to be causing this issue because the abruptness of the interfaces increases with lower doped regions implying the dispersion of P is linked to the doping concentration in the heterostructure. A plot showing the relationship between impurity concentration and dopant flow for all samples is shown in figure 6, which shows a linear relationship between the dopant flow rate and impurity concentration for all samples excluding P1 (5×10^{20} cm^{-3}). The deviation of sample

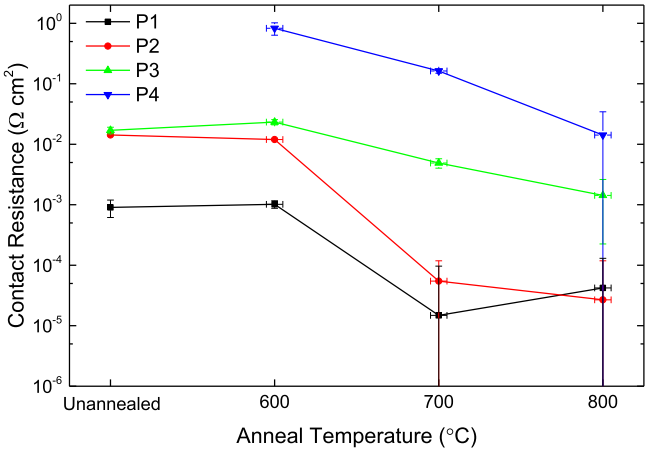

Figure 10. Showing the influence of annealing temperature on the contact resistance of NiCr contacts to the P doped 3C-SiC TLM device structures.

P1 from the linear relationship indicates a saturation of dopants in the 3C-SiC film and implies non-reacted dopant precursor must be flowing through the CVD.

The linear relationship offers accurate control of the impurity concentration of 3C-SiC up to around 1×10^{20} cm^{-3}.

3.2. Electrical activation and resistivity

Temperature dependence resistivity, in the range of 15–300 K, for samples P1-P4 are shown in figure 7, measured in the absence of a magnetic field within the variable temperature Hall system.

The resistivity of the highly doped layers is almost independent of temperature implying a very low activation energy of the P dopants as the semiconductor exhibits degenerative behaviour. Lower doped samples show more temperature dependent behaviour, as expected. Sample P4 could only be measured down to approximately 200 K as the resistance of the device reached ~50 MΩ, exceeding the capability of the measurement equipment. No reliable measurements could be extracted from sample P5 for the same reason.

The carrier concentration was extracted using the same Hall bar devices in the presence of a magnetic field over the same temperature range. The results from samples P1, P2 and P3 can be seen in figure 8. The carrier concentrations of samples P2 and P3 are in good agreement with the SIMS profiling measurements, however, P1 shows the n-type dopants have reached a saturation limit for the particular growth conditions. The room temperature electron mobility of samples P1 and P2 were approximately 6 cm^2 V^{-1} s^{-1} while the mobility of sample P3 is higher at 11 cm^2 V^{-1} s^{-1}. These values of bulk electron mobility are typical of highly doped 3C-SiC [12]. A comparison between the SIMS and Hall effect measurements can be seen in figure 9.

The results show an ideal linear relationship between the two measurements techniques for samples P2–P4 with a slight systematic shift between the measurements, likely caused by

Table 2. Comparing the impurity and carrier concentrations achieved through low temperature *in situ* doping with ion implantation and *in situ* doping of other n-type dopants in 3C-SiC.

Dopant	Growth method	Impurity concentration (cm^{-3})	Carrier concentration (cm^{-3})	Activation (%)	Reference
P	Ion implantation	6×10^{20} (SIMS)	—	—	[15]
N	Ion implantation	6×10^{20} (SIMS)	7×10^{19} (Hall)	11.7	[11]
N	Ion implantation	1×10^{20} (simulated)	6×10^{19} (Hall)	60	[16]
N	*In situ*	8×10^{18} (SIMS)	6×10^{19} (Hall)	>100	[17]
Al	*In situ*	6×10^{20} (SIMS)	2×10^{17} (Hall)	0.1	[18]
P	*In situ*	2×10^{20} (SIMS)	2×10^{20} (Hall)	100	This work

uncertainties in epilayer thicknesses or inherent uncertainty with the SIMS measurements themselves. The high error on the carrier concentration of sample P4 stems from limitations in the Hall effect measurements as the high resistance of this sample introduces large offset voltages that mask the relatively small Hall voltage. Sample P1 shows a significant discrepancy between the room temperature carrier concentration and the P impurity concentration with only ~40% of the dopants being electrically active. This implies the presence of a high number of electrically inactive interstitial impurities.

3.3. Contact resistance

Finally, the contact resistance of the NiCr contacts was analysed to assess the influence of doping and thermal annealing on the formation of low resistance Ohmic contacts. The TLM devices were subjected to annealing temperatures between 600 °C–800 °C and the contact resistance was subsequently extracted at room temperature from the devices using a four-wire configuration, see figure 10.

High temperature annealing of the NiCr contacts at 800 °C resulted in the lowest contact resistance for all samples, likely by the formation of a low resistance silicide. Both samples P1 and P2 showed contact resistance of approximately $2 \times 10^{-5}\,\Omega\,cm^2$, however, the experimental error sets this as an upper limit and the contact resistance could be significantly lower. The high errors are a result of separation uncertainty due to the photolithography process in the fabrication of the linear-TLM structures, as accurate separation could only be achieved down to 2 μm. This error could be significantly reduced with a more accurate process for fabricating smaller separations such as electron beam lithography. This contact resistance is amongst the highest reported in the literature for 3C-SiC [13, 14]. Further reduction of contact resistance may be possible with increased temperature annealing of the NiCr contacts, especially with the lower doped 3C-SiC samples.

4. Conclusions

An effective method for doping 3C-SiC epilayers grown at low temperatures with P has been demonstrated and can reliably be used to dope the material in a range from $\sim 1 \times 10^{17}\,cm^{-3}$ (and well below) up to $2 \times 10^{20}\,cm^{-3}$ with 100% electrical activation. This level of doping and activation is among the highest quoted in previous studies and activation levels using ion implantation are rarely achieved at these concentrations of impurities, see table 2. Doping *in situ* during epitaxy can simplify device fabrication processes by avoiding high energy ion implantation and high temperature thermal annealing processes to activate carriers and restore crystallinity. Doping during epitaxial growth also enables the formation of complex doping profiles and could be combined with selective epitaxy for introducing dopants into selected areas for contact formation.

While P diffusion and segregation is often a serious issue with silicon and germanium growth, the effect is limited in 3C-SiC producing relatively abrupt profiles within the doped heterostructures. An ideal, linear dependency on dopant flow rate and impurity concentration was demonstrated with 100% electrical activation up to $\sim 2 \times 10^{20}\,cm^{-3}$ within the 3C-SiC epilayers, enabling the formation of low resistance contacts and the fabrication of complex device structures with accurate control over electrical properties.

Acknowledgments

This work was supported by the EPSRC 'Platform Grant' EP/J001074/1 and in part by the University of Warwick's Higher Education Innovation Fund (HEIF).

ORCID iDs

Maksym Myronov https://orcid.org/0000-0001-7757-2187

References

[1] Ostling M *et al* 2011 *2011 IEEE 23rd Int. Symp. on Power Semiconductor Devices and ICS* p 10
[2] Wright N G and Horsfall A B 2007 SiC sensors: a review *J. Phys. D: Appl. Phys.* **40** 6345
[3] Matsunami H and Kimoto T 1997 Step-controlled epitaxial growth of SiC: high quality homoepitaxy *Mater. Sci. Eng.* R **20** 125
[4] Ferro G 2014 3C-SiC heteroepitaxial growth on silicon: the quest for holy grail *Crit. Rev. Solid State Mater. Sci.* **40** 56

[5] Lien W C *et al* 2010 Growth of epitaxial 3C-SiC films on Si(100) via low temperature SiC buffer layer *Cryst. Growth Des.* **10** 36
[6] Wang L *et al* 2011 Growth of 3C-SiC on 150 mm Si(100) substrates by alternating supply epitaxy at 1000 °C *Thin Solid Films* **519** 6443
[7] Zhuang H *et al* 2013 Low temperature hetero-epitaxial growth of 3C-SiC films on Si utilizing microwave plasma CVD *Chem. Vap. Depos.* **19** 29
[8] Jha H S and Agarwal P 2015 Highly crystalline silicon carbide thin films grown at low substrate temperature by HWCVD technique *J. Mater. Sci.: Mater. Electron.* **26** 1381
[9] Myronov M *et al* 2015 *Growing epitaxial 3c-sic on single-crystal silicon* UK Patent GB2540608A
[10] Rauls E *et al* 2003 The different behavior of nitrogen and phosphorus as n-type dopants in SiC *Physica* B **340** 184
[11] Li F *et al* 2015 Electrical activation of nitrogen heavily implanted 3C-SiC(100) *Appl. Surf. Sci.* **353** 958
[12] Piluso N *et al* 2010 Optical investigation of bulk electron mobility in 3C–SiC films on Si substrates *Appl. Phys. Lett.* **97** 142103
[13] Bazin A E *et al* 2010 Ti–Ni ohmic contacts on 3C–SiC doped by nitrogen or phosphorus implantation *Mater. Sci. Eng.* B **171** 120
[14] Wan J *et al* 2002 Formation of low resistivity ohmic contacts to n-type 3C-SiC *Solid-State Electron.* **46** 1227
[15] Battistig G *et al* 2006 A view of the implanted SiC damage by Rutherford backscattering spectroscopy, spectroscopic ellipsometry, and transmission electron microscopy *J. Appl. Phys.* **100** 093507
[16] Taguchi E *et al* 2007 *Silicon Carbide and Related Materials* (Stäfa: Trans Tech Publications) pp 579
[17] Chen J *et al* 2000 *Silicon Carbide and Related Materials* ed C H Carter *et al* (Uetikon am See: Trans Tech Publications) p 273
[18] Wang L *et al* 2011 Demonstration of p-type 3C–SiC grown on 150 mm Si(100) substrates by atomic-layer epitaxy at 1000 °C *J. Cryst. Growth* **329** 67