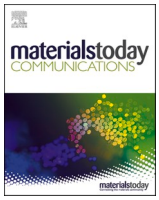
Materials Today Communications 38 (2024) 108312

Contents lists available at ScienceDirect

Materials Today Communications

journal homepage: www.elsevier.com/locate/mtcomm



Single step silicon carbide heteroepitaxy on a silicon wafer at reduced temperature

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ARTICLE INFO

Keywords:
3C-SiC
Heteroepitaxy
CVD

ABSTRACT

A single step growth approach for wafer-scale homogeneous cubic silicon carbide (3C-SiC) heteroepitaxy, using chemical vapour deposition (CVD), on a silicon (Si) substrate is demonstrated. Residual biaxial tensile strain causing a wafer bow is eliminated in the 3C-SiC epilayer via in-situ defects engineering and heteroepitaxy at reduced temperature. Thermal mismatch between the 3C-SiC epilayer and substrate is minimised by a substantial reduction of growth temperature, down to ~1000 °C. Heteroepitaxy of high quality, fully relaxed 3C-SiC epilayers with minimal wafer bow is demonstrated, made possible by careful process optimisation. Unusually very high growth rate of 3C-SiC of > 10 μm/hr is achieved. At the same time the epilayer is free from any other silicon carbide (SiC) polytype inclusions. Moreover, the reduced growth temperature unlocks the ability to deposit high quality 3C-SiC epilayers within traditional Si-based cold walled CVD reactors, enabling the growth of such thin films on unprecedently high volumes and wafer diameters up to 300 mm and above.

1. Introduction

Silicon carbide (SiC) is a wide bandgap compound semiconductor which shows high potential for the ongoing electrification of the world and creation of disruptive technologies in sensors, micro-electromechanical systems (MEMS) and harsh environment electronics and optoelectronics. The next generation of power electronics can contribute in suppressing climate change by improving the efficiency of electric power conversion, which is applicable to a range of industries and social infrastructures [1–4]. The high electric field breakdown and low switching losses of SiC make it ideal for high voltage and high frequency applications such as those found in electric vehicles. Also SiC possesses other excellent material properties at room-temperature such as high thermal conductivity (360 W $m^{-1}K^{-1}$), high hardness (9.3 Mohs hardness), and resistance to all wet and gaseous chemical etchants. It is not susceptible to damage from various forms of radiation as well. Semiconductor devices fabricated from SiC can operate at very high temperatures (>600 °C) and in harsh environments [3]. These properties make it ideal for use in various applications beyond power electronics including microwave, harsh environment sensors, MEMS and biomedical devices. Also, relaxed cubic SiC, with a lattice constant of 0.436 nm, grown on a silicon (Si) substrate, is ideal virtual substrate for subsequent epitaxy of other scientifically and technologically important materials such as gallium nitride (GaN), aluminium nitride (AlN), [5] boron nitride (BN), [6,7] boron arsenide (BAs), [8] Diamond and various 2D materials, including graphene, and thus allows their integration with Si [9,10]. Successful device technology is greatly dependent on the wafer/substrate and epitaxial material quality.

SiC exists in over 250 different crystalline forms called polytypes, see Fig. 1 [11]. The hexagonal structured 4H-SiC dominates the SiC market due to the availability of crystalline wafers up to 150–200 mm diameter and well-developed homoepitaxial growth processes. While 4H-SiC is available in commercial applications, such as power devices and substrates for GaN and other III–V materials, 4H-SiC wafers are extremely expensive and subsequent homoepitaxy requires dedicated hot-walled chemical vapour deposition (CVD) reactors operated at very high temperatures over 1650 °C, which leads to high operating and maintenance costs. Nevertheless, 4H-SiC epilayers and substrates still contain various defects and polytypes inclusions.

SiC can also exist in a cubic, zinc-blende structured polytype 3C-SiC (β-SiC), which can be stabilised at temperatures below 1410 °C. As a consequence, SiC can be deposited on a Si substrate by heteroepitaxy. 3C-SiC has many desirable properties compared to 4H-SiC such as a lower bandgap of 2.4 eV (comparing to 3.2 eV for 4H- and 6H-SiC), the highest theoretical electron mobility of ~1000 $cm^2V^{-1}s^{-1}$ at 293 K, which are beneficial for faster operation of a power MOSFET, and

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https://doi.org/10.1016/j.mtcomm.2024.108312
Received 18 December 2023; Received in revised form 30 January 2024; Accepted 4 February 2024
Available online 9 February 2024

isotropic materials properties due to cubic symmetry [12]. The tetrahedral symmetry of covalent bond in 3C-SiC and its isotropic crystalline structure make it a superior polytype choice in terms of its electronic properties compared to others. The higher symmetry results in higher theoretical values of electron mobility and saturation drift velocity, as a consequence of reduced phonon scattering. The anisotropic crystalline nature of 4H- and 6H-SiC polytypes results in variations in electron/hole mobility values depending on the choice of crystal axis; which is not an issue for 3C-SiC. The ability to grow 3C-SiC on a Si substrate integrates the compound semiconductor with the well-established Si material system and opens a wider opportunity for heterogeneous integration with other group-IV semiconductors such as germanium (Ge) or silicon germanium (SiGe) alloys [13,14]. Growing 3C-SiC on a Si substrate enables larger wafer diameters up to 300 mm and above, which are available at a fraction of the cost of 4H-SiC and of much higher quality and purity.

The first synthesis of 3C-SiC on Si(001) substrate was reported by Spitzer et al. in 1959, over 60 years ago, and much work has been carried out to improve the quality of the 3C-SiC epilayers since [15]. In that pioneering work, thermal CVD process with just methane diluted in argon was used to convert the surface of a Si wafer, via diffusion, into some form of graded and non-uniform SiC thin film at a temperature of 1300 °C. It took decades for another major step to happen towards the growth of 3C-SiC thin films. Inspired by the similarities of the crystal structures between 3C-SiC layers and Si substrate, and the maturity of Si wafer technology, Spitzer's work overlooked the fact that the considerable difference between both their lattice parameters and thermal expansion coefficients (TEC); [16] the disparities that are responsible for the large number of defects at the 3C-SiC/Si interface that, as the growth continues, also propagates through the epilayer to the surface. In 1983 Nishino et al. implemented a three step (cleaning, carbonisation, and growth at ~1350 °C) CVD process for improved quality crystalline growth [17]. Through this process, that included a buffer layer (carbonisation layer), some graded SiC seed layer would be deposited, on top of which the succeeding 3C-SiC epi layers would be grown. The inclusion of a SiC seed layer dramatically improves the crystal structure of the 3C-SiC and helps to reduce wafer bow caused by thermal mismatch. Having been considered an improvement to Nishino's three step process, in 2009 Chen et. al. introduced a four-step growth technique with no cooling periods in between, in a low pressure CVD reactor in which a (post-carbonisation) diffusion step was added to the conventional three step process [18]. This modified four-step process helps producing 3C-SiC epitaxial layers of improved crystal quality and reduces the formation of voids at the interface, which can form due to the out-diffusion of Si from the substrate.

In this work, a novel method, consisting of just single step, for growing wafer scale 3C-SiC on Si(001) wafer is demonstrated, making use of standard Si based growth technology utilising single wafer, thermal type, cold wall reduced pressure CVD (RP-CVD). This has been achieved by reducing the growth temperature and modifying other growth conditions, selection of correct precursors, understanding 3C-SiC materials properties and heteroepitaxy, and through careful process optimisation. Moreover, the process is much simpler, faster, cheaper, substantially less energy consuming and consists of just a single growth step comparing to traditional multi-steps.

2. Materials and methods

2.1. Epitaxial growth

3C-SiC epilayers of thicknesses up to ~1 μm were grown on on-axis 100 mm diameter 525 μm thick Si(001) wafers within an industrial type Si based ASM Epsilon 2000 RP-CVD cold wall system, with the capability to grow on up to 200 mm diameter wafer. It consists of a cold-walled quartz chamber, which limits an upper growth temperature to ~1200 °C and which makes achieving highly crystalline 3C-SiC a challenge. However, high throughput of these machines and significant reduction of deposition on the chamber walls would allow mass production of low-cost 3C-SiC/Si epi wafers utilising the existing network of Si-foundries. The C to Si ratio was controlled through the ratio of C to Si gaseous precursors injected into the growth chamber at reduced pressure below 200 Torr. Dichlorosilane and trimethylsilane were used as precursors. Growth rates of over 10 μm/hr were obtained. The Si wafer was loaded into the CVD growth chamber at 900 °C, as shown in Fig. 2b. Then the temperature was rapidly raised up to ~1000 °C at which native silicon oxide was thermally desorbed from the Si surface. Immediately after that the growth of 3C-SiC commenced.

In thermal CVD, the growth temperature strongly defines the suitability of a particular material's precursor for its application. *The incorrect selection of the precursor simply prohibits obtaining desired results.* The first requirement is the occurrence of thermal decomposition, by means of thermal energy, of a precursor's molecule at a given temperature. For an example, traditional C precursors propane, methane or ethylene, widely used in SiC epitaxy at temperatures above ~1350 °C are not suitable for the reduced temperature epitaxy. This is the main reason why all previous efforts to grow SiC, using such precursors, at reduced temperatures were unsuccessful. Moreover, even inefficient decomposition of the precursor prohibits achieving reasonable growth rate of an epilayer.

Initial growth processes for 3C-SiC were carried out at temperatures of ~1200 °C. To suppress the out-diffusion of Si and to create a seed layer for the subsequent epitaxy of 3C-SiC a silicon carbon alloy

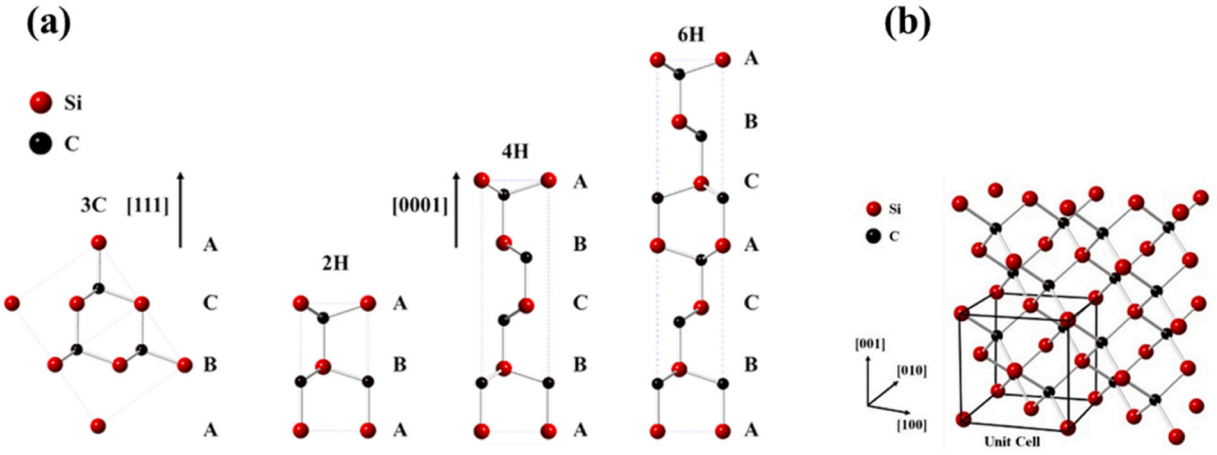

Fig. 1. a) Unit cells of SiC polytypes: 3C-SiC, 2H-SiC, 4H-SiC and 6H-SiC (left to right). (b) Cubic crystal structure of 3C-SiC showing unit cell.

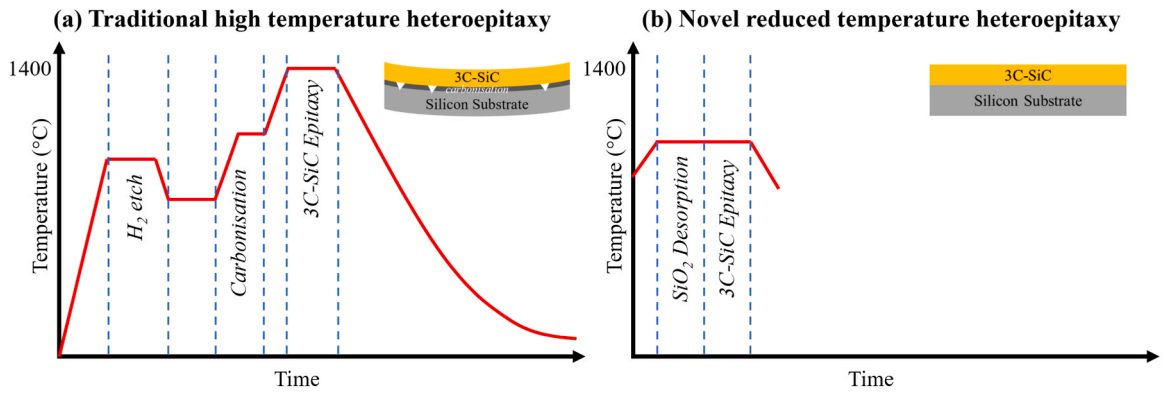

Fig. 2. Heteroepitaxy of 3C-SiC on Si. (a) State of the art multi-steps 3C-SiC heteroepitaxy. (b) Novel reduced temperature heteroepitaxy growth process showing simplified steps and dramatically shorter processing time.

($Si_{1-x}C_x$) buffer layer was deposited with approximately 1 % C composition [19]. In contrast to well established carbonisation buffer, see Fig. 2a, which creates some graded $Si_{1-x}C_x$ layer of poor quality and not even monocrystalline in the most cases, we used to innovation and introduced a defect free $Si_{1-x}C_x$ alloy epilayer lattice matched to Si, which maintains the same crystallinity as Si substrate. As the growth process was further optimised, the deposition temperature was reduced to ~1000 °C at which point the out-diffusion of Si could be suppressed through optimising the C/Si ratio in the growth phase and as a result the $Si_{1-x}C_x$ buffer layer was found to be unnecessary and a simplified process could be used, as shown in Fig. 2b. However, it could indeed be used as a seed layer for traditional high temperature 3C-SiC heteroepitaxy on Si.

The same occurred with our initial trials on on-axis and off-axis Si (001) substrates. Due to reduced growth temperatures, traditionally used off-axis Si substrates are unnecessary, as was expected, and therefore standard and commonly used on-axis substrates can be used. It is very beneficial for electronic devices applications, because presence of surface steps in the off-axis substrate generally degrades most of a device's performance.

2.2. Materials characterisation

The grown 3C-SiC epi wafers were characterised using a range of techniques discussed below. The crystalline states of the grown 3C-SiC epilayers were verified using standard high resolution X-ray diffraction (HR-XRD) ω-2θ rocking curves and reciprocal space maps (RSMs) carried out on a Panalytical X'Pert MRD diffractometer with $CuK\alpha_1$ radiation. HR-XRD can quantify the crystal quality of the epilayer and assess whether the films are monocrystalline, polycrystalline, amorphous and under significant levels of tilt or residual strain. Atomic Force Microscopy (AFM) was performed on as grown samples to determine the surface morphology and roughness using a Bruker Icon AFM operating in Scan assist mode. Cross-sectional transmission electron microscopy (X-TEM) is one of the most effective techniques to assess the crystallinity and morphology of 3C-SiC epilayers. When preparing electron transparent samples for X-TEM, traditional mechanical grinding and Ar beam milling are effective on 3C-SiC epilayers below ~1 μm thick and more complex extraction techniques such as focussed ion-beam (FIB) can be avoided. X-TEM samples were prepared through the use of SiC grinding pads and Ar ion polishing and X-TEM micrographs were obtained on a JEOL 2100 TEM. Thickness uniformity measurements were performed on a Bruker Vertex V70 FTIR and wafer bow measurements were obtained on a Bruker DektakXT stylus profiler.

All presented results were obtained from 3C-SiC epilayers grown on 100 mm diameter and standard thickness of 525 μm on-axis Si(001) wafers.

3. Results and discussion

3.1. C/Si Ratio

After the selection of appropriate precursors, the C/Si ratio must be adjusted in order to grow a high quality 3C-SiC compound epilayer, but not a $Si_{1-x}C_x$ alloy [19] or SiC compound with high density of interstitial Si or C defects. Correct C to Si ratio is *absolutely essential to obtain SiC compound of any polytype including 3C-SiC*. Thermal decomposition of any Si or C precursor depends on the bonding energy of a particular precursor molecule and therefore could create more or less Si or C atoms emerging on the substrate's surface. A 3C-SiC epilayer grown under optimum growth conditions exhibits the lowest surface roughness and the highest crystal quality. Characterisation results from samples growth with reduced, optimal and increased C/Si ratios can be seen in Fig. 3. Non-optimal growth conditions produce very high surface roughness implying poor island growth mechanisms with high levels of interstitials, however, at optimal C/Si ratio a very low RMS of ~3 nm can be achieved, which results in a mirror-like surface of the 3C-SiC/Si(001) epi wafer, see Fig. 7.

When the C/Si ratio is low, no 3C-SiC epilayer Bragg peaks at (002) and (004) reflections in ω-2Θ scan are visible implying that the grown film is polycrystalline or amorphous and a sufficient level of C is required to initiate monocrystalline epitaxy. Growth of 3C-SiC grown using an optimal C/Si ratio resulted in the strongest Bragg peaks at (002) and (004) reflections with the lowest FWHM suggesting highly crystalline 3C-SiC. No polycrystalline peaks are observed in the ω-2Θ scan. When the C/Si ratio is higher than optimal, the 3C-SiC remains crystalline with only a slight reduction in peak intensities and broadening of FWHMs suggesting an excess of C in the growth phase has only a minor impact on crystal quality. Therefore, the structure of the 3C-SiC thin films varies dramatically with C/Si ratio and characterisation results obtained with AFM, XRD and XTEM, shown in Fig. 3, correlates very well. When the C/Si ratio is non-optimal, poor crystallinity is observed in the films and extremely rough surface morphology implies 3D island growth modes. For low C/Si ratio the 3C-SiC thin film is polycrystalline. For optimal C/Si ratio, the epilayer is observed to be crystalline throughout, with smooth surface, abrupt 3C-SiC epilayer and the Si(001) substrate interface. Also, voids formation in the Si substrate is completely eliminated, even without the inclusion of a buffer layer or carbonisation. More details of the C/Si ratio impact on the materials properties of the 3C-SiC thin films will be published elsewhere.

3.2. Growth rate

In order to achieve true continuous thin film deposition by CVD, the 3C-SiC growth rate has to be maximised and adjusted. Growth of any semiconductor alloy or a compound, consisting of two or more

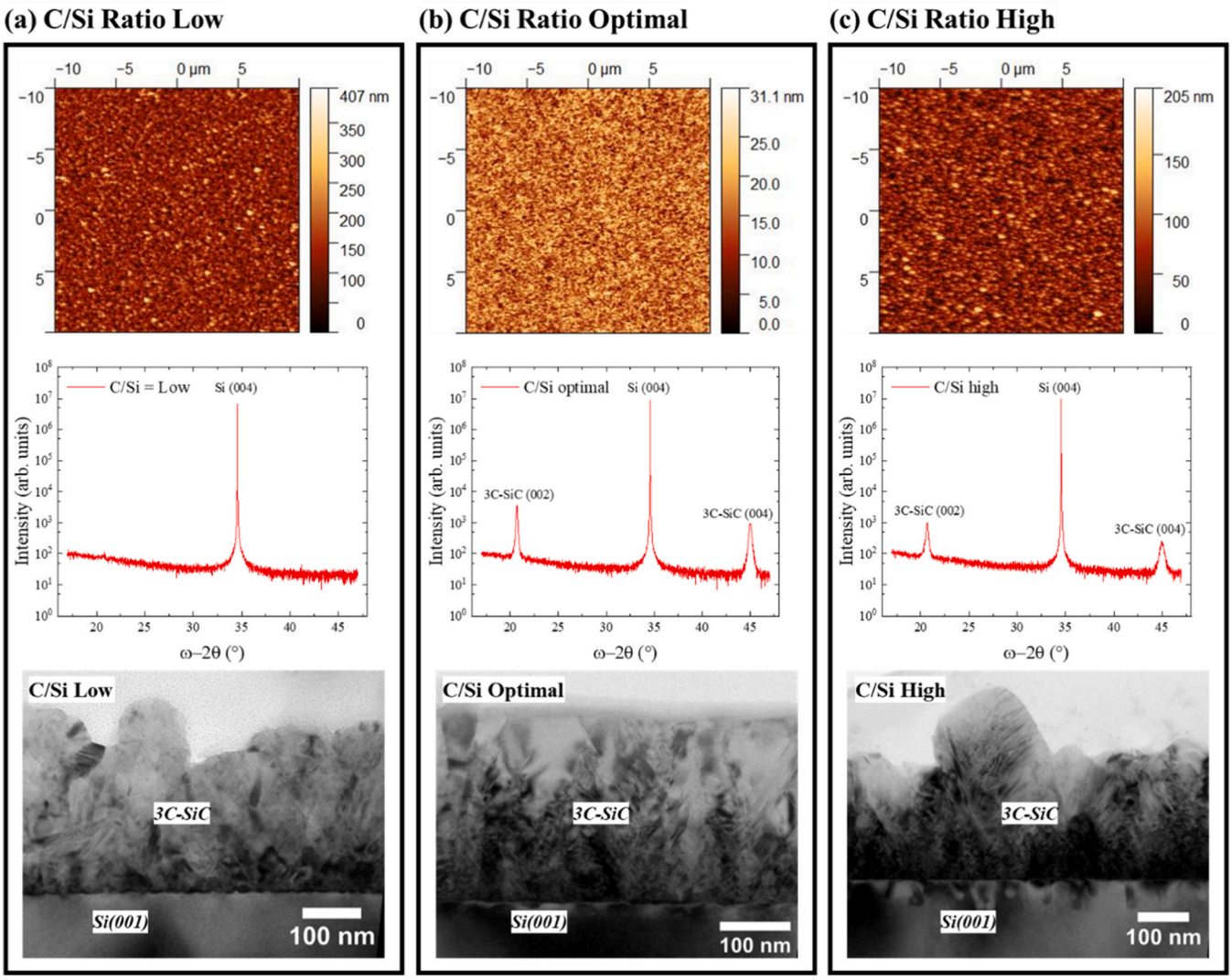

Fig. 3. Influence of C/Si ratio on the properties of 3C-SiC epilayers showing surface morphology with AFM maps, crystallinity with HR-XRD coupled scans and structure and defect formation in X-TEM micrographs for low, optimal and high C/Si ratios.

dissimilar materials, is very challenging by strong segregation effects caused by one of the materials. In the case of 3C-SiC, C segregates over Si, and therefore struggles to incorporate into the 3C-SiC lattice structure as a substitutional atom. There are two main strategies to overcome this issue and suppress the segregation effect, - via simultaneous reduction of growth temperature and maximising the epilayer's growth rate [19]. In addition to reducing the growth temperature, reasons for which have already been outlined above, the 3C-SiC growth rate has to be substantially increased then. So far, we have achieved the growth rate of 3C-SiC above 10 μm/h. This is an extremely high growth rate for low-temperature epitaxy, and comparable to traditional and well-established high temperature heteroepitaxial growth of 3C-SiC and homoepitaxial growth of 4H-SiC [11]. Also, such a high growth rate is essential for the epitaxial growth of thick SiC thin films structures, i.e. in the range of 1 to 100 μm, with varied doping type and level used to fabricate various power electronic devices. However, in contrast to it, sensor devices require substantially less than 1 μm thick 3C-SiC epilayers. Nevertheless, our results indicate that we have not achieved the maximum growth rate of the 3C-SiC yet, which opens great opportunities for further research and development.

3.3. Crystallinity, state of strain and defects

A typical HR-XRD RSMs obtained on a high quality, i.e. grown with optimal C/Si ratio, 3C-SiC/Si(001) epi wafer are shown in Fig. 4. They proof that the 3C-SiC epilayer is free of any tilt relative to the Si(001) substrate and is under only a slight residual tensile strain of < 0.1 %. Analysis of the RSMs shows both in-plane and out of plane lattice constants of the 3C-SiC are the same, i.e. ~0.436 nm, indicating the epilayer is fully relaxed. Moreover, Fig. 4c shows ω rocking curve, which was obtained around the 3C-SiC(002) Bragg peak for the 300 nm thick epilayer and its FWHM found to be 0.98°. The broadening of the peak appears due to presence of defects in the epilayer, but it is comparable to the values obtained in 3C-SiC layers grown at higher temperatures [11]. Growing thicker epilayer would decrease the defect density and reduce the FWHM of the film. It is necessary to point out that full relaxation of the 3C-SiC epilayer is achieved in very thin and just 300 nm thick epilayer.

3.4. Lattice imaging

Lattice resolved X-TEM micrographs of the 3C-SiC surface and 3C-SiC/Si(001) interface from a high quality 3C-SiC/Si epi wafers grown using optimal C/Si ratio are shown in Fig. 5. The micrograph from the

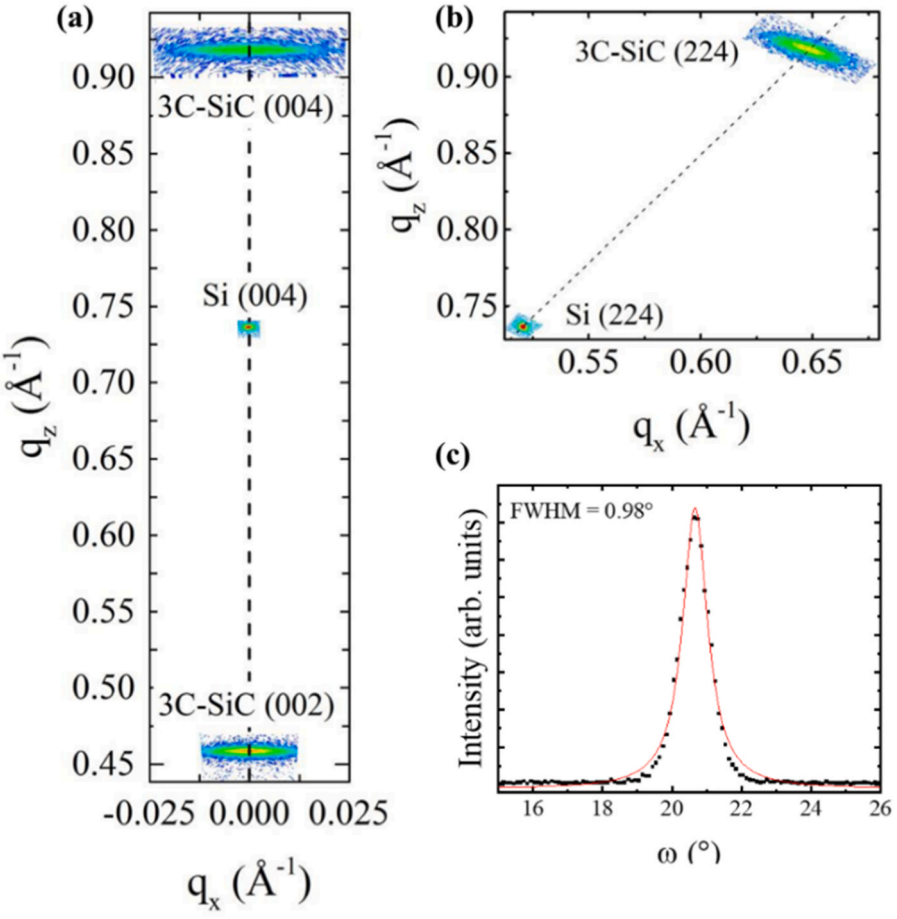

Fig. 4. HR-XRD RSMs. (a) Symmetrical (004) and (b) asymmetrical (224) RSMs of a 300 nm thick 3C-SiC/Si(001) epi wafer grown using an optimal C/Si ratio. (c) FWHM of the 3C-SiC(002) Bragg Peak. Symmetrical RSM indicates absence of 3C-SiC epilayer tilt, while the asymmetrical RSM clearly visualise absence of substantial residual strain in the 3C-SiC epilayer.

3C-SiC/Si interface shows the insertion of additional atomic planes corresponding to the expected 1-in-5 ratio, however, at the surface of even a relatively thin 300 nm thick epilayer, the defect density is reduced significantly, resulting in areas of perfect 3C-SiC crystal structure (Fig. 5a). Selective area electron diffraction (SAED) patterns confirm that the entire 3C-SiC epilayer is monocrystalline, with no signs of any polycrystalline of amorphous inclusions (Fig. 5c). A high density of stacking faults is found at the 3C-SiC/Si interface, however, this rapidly decreases due to annihilation, see Fig. 5d. Its density decreases from $\sim 16 \times 10^5$ cm^{-1}, in 3C-SiC epilayer at ~50 nm distance from the 3C-SiC/Si(001) interface, to $\sim 4 \times 10^5$ cm^{-1} near the surface of the 300 nm thick 3C-SiC epilayer.

3.5. Wafer bow

Almost full strain relaxation, or in other words very small residual tensile strain, i.e. < 0.1 %, occurs within the 3C-SiC epilayer, grown with optimum C/Si ratio, which suppresses the wafer bow. As an example, Fig. 6 shows the wafer bow of a 100 mm diameter 3C-SiC/Si (001) epi wafer with 300 nm 3C-SiC epilayer. Only very small warp can be observed in the 3C-SiC/Si epi wafer which is below < 20 μm at its maximum. This level of wafer warp is expected in Si substrates and hence the addition of the low temperature grown 3C-SiC epilayer has had little to no effect on the bow of the wafer. The typical acceptable wafer bow for a wafer to be processed for subsequent semiconductor device fabrication by, for an example, a lithography equipment is up to ~250 μm and for high resolution lithography processes even less bow, of < 50 μm, can be tolerated. The 3C-SiC epi wafer shown above is well below this limit and is therefore suitable for all subsequent processing steps. It is interesting to note, that the reduced temperature process also opens the possibility to grow 3C-SiC on much thinner Si wafers, i.e. ~200 μm, which are essential for MEMS, sensors and photovoltaic devices applications or others where the thin Si wafer is essential or Si wafer has to be etched partially or completely.

3.6. Thickness Uniformity

Superior 3C-SiC epilayer's uniformity across a full wafer is demonstrated as well, which is essential for mass production and high yield. Fig. 7a shows FTIR reflectance spectrum for a 300 nm thick 3C-SiC epilayer. Fig. 7b shows 2D thickness map of 3C-SiC epilayer with thickness uniformity of < 1.5 % across 100 mm wafer. Epi wafers of varying 3C-SiC epilayer thickness from 100 up to 800 nm exhibits superior uniformity visible due to colour variation of wide band gap 3C-SiC epilayer grown on Si, as shown on Fig. 7c.

3.7. Importance of reduced growth temperature

The 3C-SiC is the most thermodynamically stable of all SiC polytypes at low temperatures, which means at relatively low temperature growth i.e. $<$ ~1250 °C no other polytypes apart from 3C-SiC will be present. Increasing the growth temperature of 3C-SiC often leads to improved quality and lower defect densities, however, lower growth temperatures are desirable as they reduce the thermal mismatch between the 3C-SiC and Si substrate. Wafer bow is a common issue with 3C-SiC/Si epi wafers and is caused by the high thermal mismatch between the 2

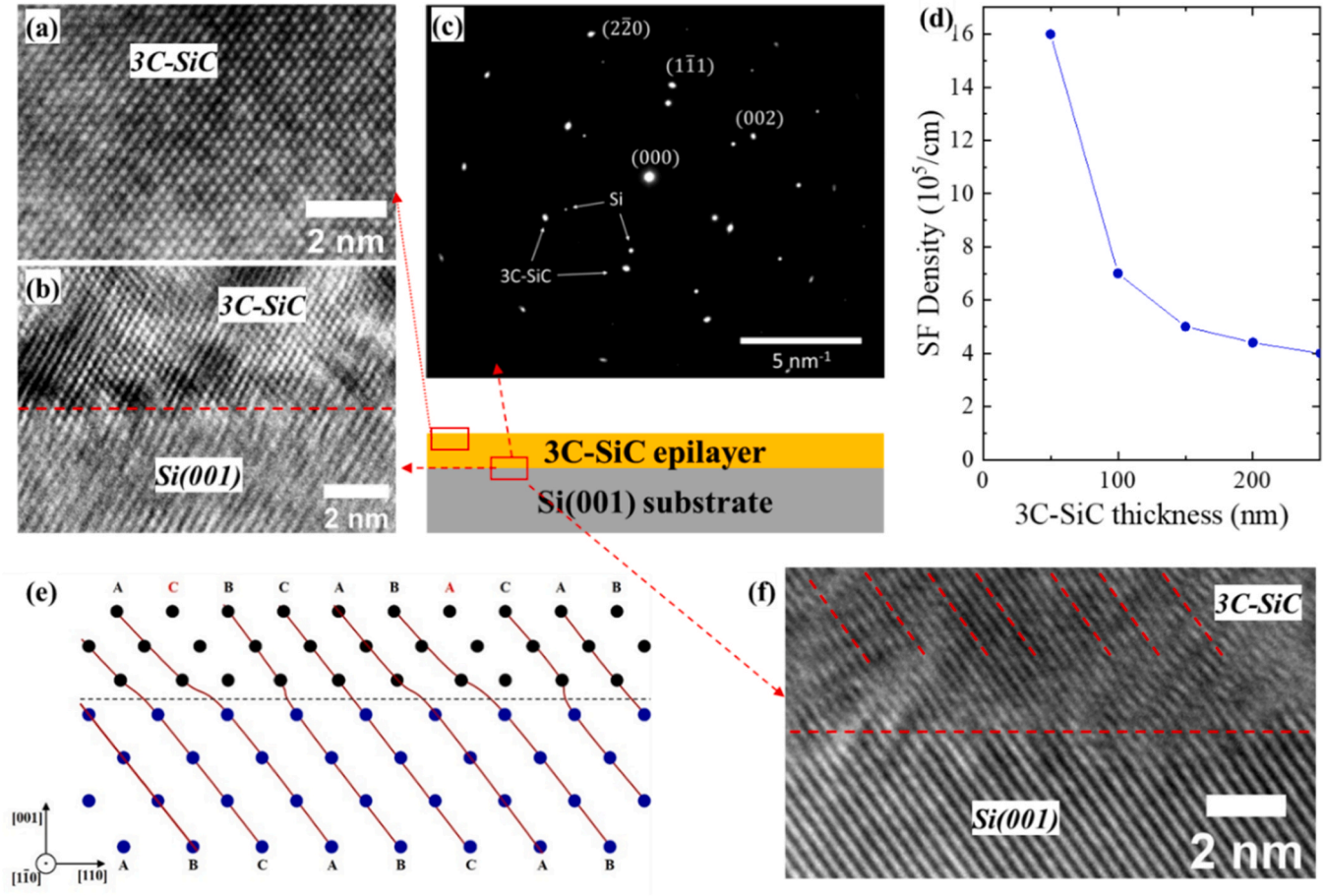

Fig. 5. X-TEM Analysis. Lattice resolved X-TEM micrographs of the 3C-SiC surface (a) and 3C-SiC/Si interface (b) from a high quality 3C-SiC/Si epi wafers grown using optimal C/Si ratio. (c) SAED pattern from the 3C-SiC/Si interface. (d) Measured linear stacking fault density as a function of epilayer thickness from X-TEM images. (e) Crystal structure schematic showing inserted dislocations every 1/5 plane corresponding to a 20 % lattice mismatch. (f) defocused X-TEM micrograph at 3C-SiC/Si interface showing the additional inserted misfit dislocations.

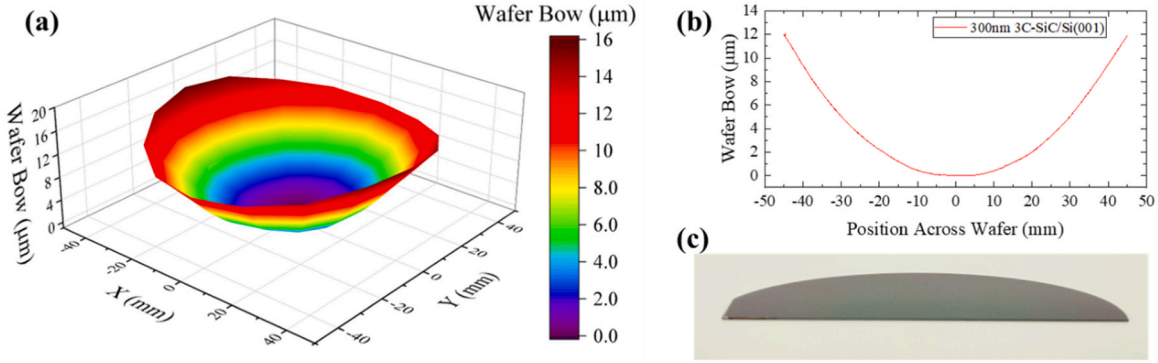

Fig. 6. Wafer Bow. (a) 3D map of wafer distortion across a 300 nm thick 3C-SiC epilayer grown on a standard 525 μm thick 100 mm diameter Si(001) substrate. (b) Line scan showing wafer bow across the 300 nm 3C-SiC/Si(001) diameter. (c) The resulting 3C-SiC epi wafer is completely flat and no bow is observable optically. The typical acceptable wafer bow for a wafer to be processed for subsequent semiconductor device fabrication by, for an example, a lithography equipment is up to ~250 μm and for high resolution lithography processes even less bow can be tolerated (<50 μm).

dissimilar materials, introducing a high level of stress into the epilayer and makes the material unsuitable for semiconductor device micro- and nano-fabrication techniques where wafer bow is a critical parameter. Due to enormous wafer bow and very poor material quality the 3C-SiC/Si wafers, even up to 100 mm diameter, cannot be processed to manufacture any reliable electronic devices. *And therefore, there is still no any commercial and mass produces power electronic or any other devices made from 3C-SiC/Si epi wafers.* Another issue with 3C-SiC heteroepitaxy is caused by its huge lattice mismatch, of 19.7 % at 293 K, with Si, which results in the insertion of misfit dislocations at every 5th 3C-SiC plane [20]. This results in the formation of various planar defects such as stacking faults and microtwins which propagate up through the 3C-SiC epilayer. Additionally, the difference in TEC between 3C-SiC epilayer and Si and residual strain in the epilayer can lead to serious wafer bow,

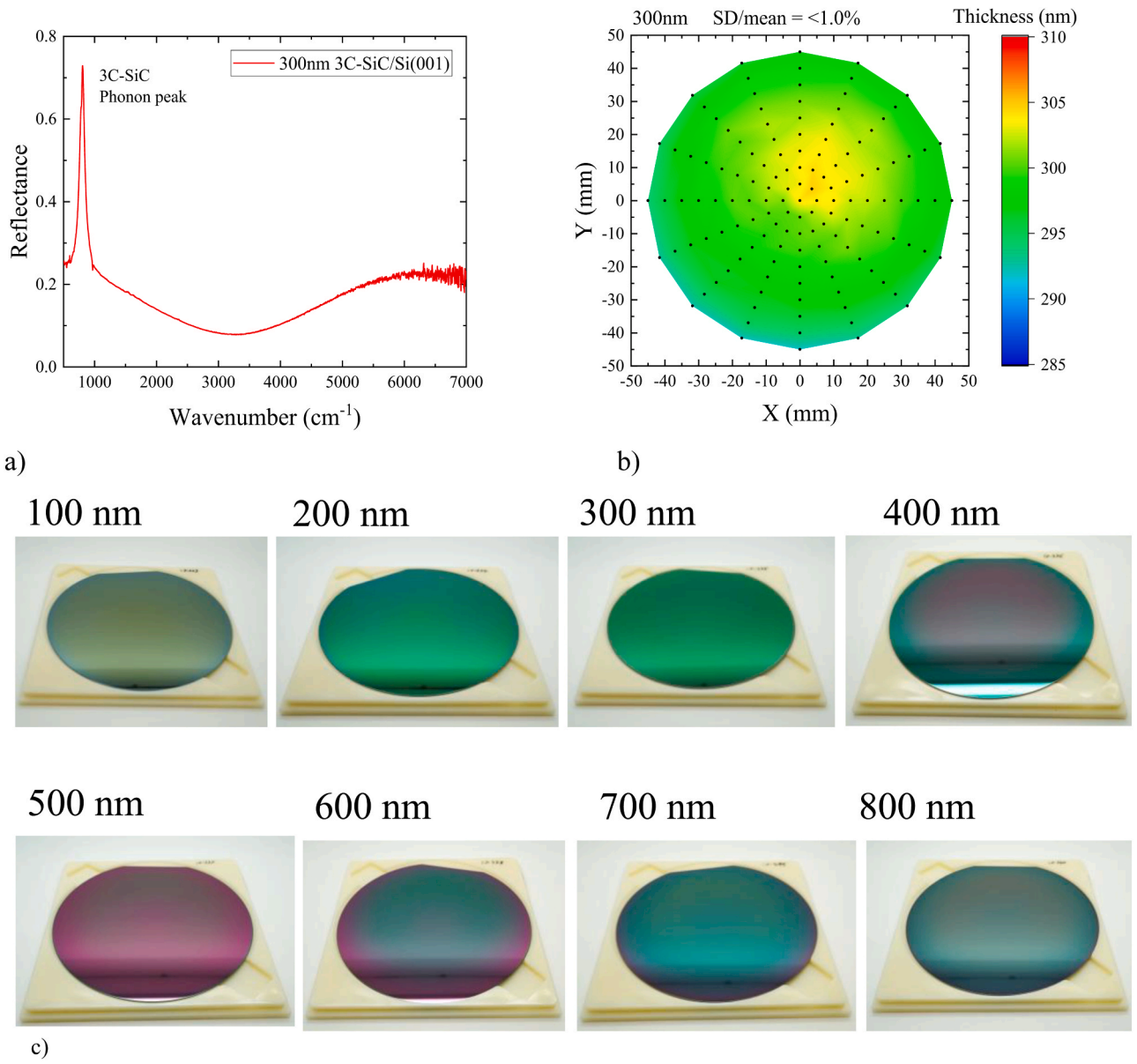

Fig. 7. Wafer uniformity. (a) FTIR reflectance spectrum for a 300 nm thick 3C-SiC epilayer. (b). Wafer uniformity of a 100 mm 3C-SiC epi wafer showing uniformity of < 1.0 % across 90 % of the wafer diameter. (c) Epi wafers of various 3C-SiC epilayer thickness exhibits superior uniformity visible due to colour variation of wide band gap 3C-SiC epilayer grown on Si.

which increases with epilayer thickness and growth temperature [21]. As 3C-SiC lacks inversion symmetry, heteroepitaxy can also lead to the formation of anti-phase domains (APDs), however, this can be suppressed through the growth on off-axis Si substrates.

Since the major breakthrough of the carbonisation step, devised by Nishino et al., [17] almost all 3C-SiC heteroepitaxy on Si has relied on a buffer layer between the substrate and epilayer to suppress out-diffusion of Si, from the Si wafer, and suppress the effects of the lattice mismatch. The growth of 3C-SiC is usually performed at a final growth temperature of 1350–1400 °C, within specialised hot wall SiC RP-CVD reactors using either single or multi source precursors for Si and C. Any research group or company looking to grow 3C-SiC/Si on a batch or industrial scale presently requires large investment into new reactors purposely built for the epitaxial growth of SiC, which requires high maintenance and reduced growth capabilities. Due to the immaturity of SiC based reactors, most are not designed with high temperature un/loading capabilities and as such each growth run must start at room temperature and be cooled fully before unloading a wafer, which adds significant time to growth runs which can exceed 6 h per wafer. Therefore, the best high temperature growth processes now involve multiple growth stages [18,22,23]. 3C-SiC quality increases with epilayer's thickness as stacking faults annihilate, however, after decades of research, 3C-SiC grown on Si is still to penetrate the commercial market as the process for growing 3C-SiC on Si is plagued with various issues such as very high growth temperatures, thermal stresses, high cost, very poor epitaxial material quality and poor scalability. While these growth methods can offer crystalline 3C-SiC, wafers still suffer from significant wafer bow due to the high growth temperature and residual strain in the epilayer [24]. This fact alone prevents the wafer scale production of 3C-SiC based devices using standard wafer processing techniques. In addition, 3C-SiC material quality is very poor, i.e. surface roughness is very high, usually > 50 nm RMS, and requires subsequent planarization using CMP in order to obtain smooth surface, particles on a surface, existence of voids at the SiC/Si interface, inclusion of various polytypes apart from the 3C-SiC, incomplete relaxation of the 3C-SiC thin film, and issues with growing intrinsic epilayers and both n- and p-type doping, etc [8].

Growing 3C-SiC at lower temperatures, i.e. < 1200 °C offers various advantages such as reduced thermal stresses, the ability to grow on other substrates such as silicon-on-insulator (SOI) or even SiO_2 patterned wafers for selective epitaxy. Crucially this temperature is within the range of the existing cold-walled CVD reactors used across the Si-industry, which are based on a much more mature technology enabling faster growth at significantly reduced maintenance and costs. Reduced growth temperature by thermal CVD, at temperatures below 1200 °C, has never been able to produce high quality 3C-SiC epilayers [12,25] unless combined with an exotic processes such as microwave plasma enhanced, hot-wire or atomic layer deposition (ALD) growth sequences [26–28]. These processes are limited in their scalability both in terms of growth rate and wafer diameter and still require bespoke reactors.

Reducing the 3C-SiC growth temperature is absolutely essential to suppress wafer bow which is predominantly caused by the thermal expansion coefficient mismatch between the 3C-SiC epilayer and the substrate from growth temperature down to room temperature. This mismatch decreases as the growth temperature of the 3C-SiC epilayer is reduced. One of the biggest issues in the epitaxial growth of 3C-SiC is the material's inhomogeneity caused by a very high density of defects, presence of various SiC polytypes, anti-phase boundaries and voids at the epilayer/substrate interface. *Also, the existence of various transition SiC-like layers, discussed before, with varied SiC stoichiometry makes this situation even worse.* It is very well known that at growth temperatures above ~1300 °C [29] many of the 250, SiC polytypes can be formed inside the SiC epilayer, which leads to defects and inclusions of other polytypes within the desired crystal structure. This effect is entirely suppressed with growth temperatures < 1200 °C as only the cubic structured 3C-SiC can stabilise at such low temperatures. Also, voids at the epilayer/substrate interface occur due to Si evaporation from the substrate's surface during the initial stages of epitaxy at high growth temperature. And finally, the reduction of growth temperature will promote the generation of stacking faults in the 3C-SiC epilayer which are essential to achieve complete strain relaxation within relatively thin epilayer, as demonstrated in this work.

Therefore, to mitigate all the issues listed above, the 3C-SiC growth temperature was reduced to ~1000 °C, which is within the limitations of Si-based cold-walled RP-CVD systems.

The growth of 3C-SiC within a cold-walled RP-CVD reactor at reduced temperature unlocks another very important innovation as the Si wafer is loaded into the CVD chamber at ~900 °C and the grown 3C-SiC/Si epi wafer could be unloaded at the same temperature. The latter step is crucial in order to mitigate the issue of thermal mismatch. Also, loading and unloading the wafer at such high temperature, which is very close to growth temperature, substantially reduces the overall process time which is important for mass-scale production, reducing the entire growth process to < 30 mins for thin epilayers.

We demonstrate unprecedently high throughput 3C-SiC epi wafer scale production technology, which is achieved not only via high growth rate, but also the capability to load and unload wafers at elevated temperatures. *In addition, the reduced growth temperature significantly reduces the energy consumption for each SiC epi wafer. As a result, it could be reduced by at least one order of magnitude, which makes a very positive impact on environment and world-wide effort on reduction of CO_2 emission.*

3.8. Unlocking new opportunities for devices applications and integration

The approach to wafer scale homogeneous SiC heteroepitaxy on Si unlocks a long awaiting materials development for a wide variety of solid-state devices and their subsequent *wafer scale fabrication in large volumes and at very low costs comparable to dominating Si devices*. Thanks to low-temperature growth, the SiC epilayers can be grown either intrinsic or in-situ doped, with traditional to Si epitaxy p- or n-type dopants, resulting in electrically active impurities up to ~1×10^{20} cm^{-3} [30]. This unlocks reliable control of the SiC thin film electrical resistivity, which is essential for fabrication of any electronic device. The proposed material technology opens an opportunity for the invention of novel electronic; photonic; sensor; biomedical; energy storage, harvesting and generation; and MEMS devices with potential disruptive properties, and a long-awaiting low-cost mass production of SiC heterostructures for power electronics, sensor and other industries applications on large diameter Si wafers, up to 300 (450) mm diameter, by the existing network of semiconductor's industry cold wall CVD equipment.

Unprecedently high growth rate of 3C-SiC thin film, up to ~10 μm/h, could grow very thick epilayers in the range of ~1 to 100 μm, essential for power electronic devices. Power electronics based on SiC can greatly reduce the power losses in most generation and distribution systems for electrical energy, including ones for electric vehicles, ships, robots, drones and airplanes. The higher frequency, smaller dimensions, reduced cooling requirements, and greater efficiency obtained with SiC power electronics give more efficient systems in any applications where the AC-DC, DC-AC, or DC-DC conversions are required.

In contrast to thicker epilayers, a large variety of sensor technologies, including quantum ones, will benefit from much thinner epilayers with thickness in the range from few up to 100's nm. Also, thinner epilayers could be used to create SiC CMOS suitable for high temperature operations, i.e. above ~150 °C. It is worth noting again that due to the superior properties of SiC all these mentioned devices could be used in harsh environments, i.e. at elevated temperatures, corrosive and radiation environment, withstand sudden changes in pressure, mechanical shock etc. MEMS technology will benefit from compatibility with Si and superior selectivity of SiC to other materials. In spite of defects, the 3C-SiC layers have unique applications in MEMS operating in harsh environments. The high melting point and chemical inertness as well as the ability to selectively etch away the Si substrate to form freestanding 3C-SiC structures and sensors gives 3C-SiC a unique advantage over other materials and SiC polytypes [31]. Standard Si and SOI CMOS wafers will benefit from just their backside coating with the 3C-SiC for improved thermal dissipation, mechanical strength and as a protective mask layer during any processing or applications in harsh environment. Moreover, all these devices could be heterogeneously integrated with existing Si based devices technologies including all group-IV semiconductors like SiGe, GeSn etc., via selective epitaxy. And finally, if necessary for a particular application, then the underlying Si substrate could be completely etched away from a fabricated 3C-SiC/Si device via standard wet etchants.

The reduced temperature growth 3C-SiC also offers various mass volume device applications such as suspended membranes for optical/X-ray windows, X-TEM sample supports or forming the basis of pressure sensors. Other MEMS devices such as suspended cantilevers and wires can be used for sensing of various parameters such as temperature, chemical species, gas flow and more. The addition of in-situ doping opens the possibility to more complex device structures such as P-i-N UV photodiodes, MOSFETs and other power electronic devices.

Intrinsic or doped 3C-SiC/Si epiwafer or substrate could be used as a strain tuning platform or a virtual substrate for heteroepitaxy of foreign materials on Si via fully relaxed 3C-SiC buffer with in plane lattice constant of 0.436 nm. They include not only semiconductors, but also oxides, multiferroics and ferroelectrics. For many of them, native substrates simply do not exist, which prohibits even homoepitaxy. The inertness of SiC also acts as a diffusion barrier of foreign materials species into Si substrate or vice versa which offers great advantages for the growth of materials for radio frequency applications such as AlN and GaN. Virtual substrate is a relaxed buffer of a material epilayer, with bulk like lattice parameters, grown on an underlying substrate. Substrate can be any material as well as the relaxed buffer. Thus, the virtual substrate is a strain tuning platform for the subsequently grown epilayers. In semiconductors, the virtual substrate is used for heterogeneous integration of various semiconductor materials and oxides on the same Si platform. Over the years we invented, researched and developed a number of such virtual substrates. Some of them are already in

production. As an example, SiGe, Ge, GeSn or GeSnSi VS are used as a strain tuning platform for materials with a lattice constant larger than Si [13,32–35]. They include not only the group IV semiconductors, but also III-V compounds including GaP, AlP, GaAs, InGaAs, InSb and many others. In contrast to them there is only one strain tuning platform for materials with lattice constant smaller than Si. And it is 3C-SiC/Si virtual substrate. It could be a pathway for heteroepitaxy of diamond on Si, as it reduces the enormous 34.3 % lattice mismatch between diamond and Si to ~15 %, at 293 K. The same approach could be used for growth of emerging cubic boron nitride (c-BN) [6] and cubic boron arsenide (c-BAs) [8]. Other well researched and technologically important materials with much smaller lattice mismatch like cubic AlN, GaN, AlGaN and others could be heteroepitaxially grown on 3C-SiC/Si(001) virtual substrate.

The proposed epitaxial process is also transferable to other Si substrate orientations including Si(111), which offers a template for hexagonal materials such as AlN and GaN. 3C-SiC/Si(111) virtual substrates provide a low-cost and large diameter alternative to 4H-SiC substrates for GaN devices, including RF communications, power devices and LEDs while still offering the same low lattice mismatch of just 3.4 %, low diffusivity of impurities and high thermal conductivity. Finally, the 3C-SiC/Si virtual substrate can be used for heteroepitaxy of Graphene and other 2D materials.

4. Conclusions

In conclusion, the novel approach reported here has created a technology, which allows not only wafer scale homogeneous 3C-SiC heteroepitaxy on on-axis Si(001) wafer, but also beyond state of the art 3C-SiC epitaxial material quality. Moreover, the process is much simpler, faster, cheaper, substantially less energy consuming and consists of just a single growth step comparing to traditional multi-steps. High quality 3C-SiC epilayers can be grown at low temperatures down to ~1000 °C without the requirement for carbonisation or other buffer layers. High growth rates of above 10 μm/hr are achievable, which would enable the growth of very thin and very thick epilayers from 10's nm up to 10's μm covering a wide range of applications. High crystallinity, low surface roughness, minimal wafer bow and excellent uniformity both across each wafer and from run to run is achieved with this technique. Crucially the process can be run in a Si-based cold-walled CVD system. The process is comparable to standard Si epitaxy and offers 3C-SiC growth at a similar cost point and scale. Various other technologies are also unlocked within such reactors and reduced growth temperatures, including selective epitaxy on SiO_2 patterned substrates, blanket growth on SOI wafers and integration with other technologically important Group IV semiconductors.

Declaration of Competing Interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Maksym Myronov has patent #Patent No.: US 10,907,273 B2 issued to Maksym Myronov and Gerard Colston. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

The authors thank to Dr Alan Burton for technical support of the epitaxy and characterisation equipment and the clean room.

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