Experimental and physics-based modeling assessment of strain induced mobility enhancement in FinFETs

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Abstract
This study combines direct measurements of channel strain, electrical mobility measurements and a rigorous modeling approach to provide insight about the strain induced mobility enhancement in FinFETs and guidelines for the device optimization. Good agreement between simulated and measured mobility is obtained using strain components measured directly at device level by a novel technique. A large vertical compressive strain is observed in FinFETs and the simulations show that this helps recover the electron mobility disadvantage of the (110) FinFETs lateral interfaces w.r.t. (100) interfaces, with no degradation of the hole mobility. The model is then used to systematically explore the impact of the fin-width, fin-height and fin-length stress components on n- and p-FinFETs mobility and to identify optimal stress configurations.

Introduction
FinFETs enable scaling of CMOS by enhancing electrostatic control [1, 2, 3], and strain is an important technology booster [3, 4, 5]. Strain induced mobility enhancement in planar MOSFETs has been studied extensively [6, 7, 8, 9], but the complex stress configurations in FinFETs, consisting of \( T_{HH} \), \( T_{HI} \) and \( T_{IW} \) components (see Fig.1), still demand physics-based models to support device design. In fact, so far the stress configurations in FinFETs have been typically inferred from process simulations and the analysis of mobility data has been based on the piezo-resistive coefficients [3, 4, 10], that offer limited insight and are inaccurate at high stress [11] and for complex stress configurations as in Fig.1. Furthermore, for narrow fins, mobility data is limited and strain measurement is challenging for established techniques [12, 13]. This paper presents an assessment of the strain induced mobility enhancement based on direct strain measurements, electrical mobility measurements and numerical physics-based modeling. Mobilities in narrow n- and p-FinFETs, measured from 77K to 300K, are compared with a state-of-the-art transport model based on the Boltzmann Transport Equation (BTE) in inversion layers, accounting for all the relevant scattering mechanisms, in which strain is implicitly introduced by modification of the band structure. Simulations are then used to clarify the physical mechanisms for mobility enhancement and to provide guidelines for the device optimization.

Device fabrication and characterization
22nm node FinFETs were fabricated using a VLSI-compatible process [1, 2] (Fig.2). Strain components \( \varepsilon_{zz} \), \( \varepsilon_{yy} \) (\( z, y \) being the fin-height and fin-width directions, see DCS in Fig.1) of fully-processed devices were quantified directly by holographic interferometry [14, 15] (Figs.3 and 4). This novel technique is capable of measuring strain with nanometer spatial resolution and for relatively thick samples, thus suppressing the influence of sample relaxation. Measured \( \varepsilon_{zz} \) is very large, especially w.r.t. the low intrinsic stress of the TiN (Fig.5(a)), but it is consistent with strain induced by differences in thermal expansion coefficients following plastic relaxation at high temperature (Fig.5(b)). Mobility was extracted in 10µm long, 65nm tall FinFET devices consisting of 10 fins in parallel by split \( C-V \) and \( I-V \) measurements. The drain current was measured at \( V_{DS}=10\text{mV} \) and corrected for gate leakage current, while the inversion charge \( N_{inv} \) was obtained by integration of the gate-to-channel capacitance curve; the channel area was obtained as \( \frac{1}{2} \cdot L_{fin} \cdot (2H_{fin}+W_{fin}) \). Due to excessive gate leakage current, at \( N_{inv} \), larger than approximately \( 2 \cdot 10^{13} \text{cm}^{-2} \) the extracted mobility data were not considered to be reliable. Figs.6 and 7 compare the electron and hole mobility to literature data. Electron mobility is significantly larger than for planar MOSFETs in the \( N_{inv} \) range of interest (\( \geq 2\cdot10^{12} \text{cm}^{-2} \)). At low \( N_{inv} \) values the measured mobility shows a clear roll-off, stronger than in the reference data, most likely due to scattering by Coulomb centers in the high-\( \kappa \) stack [16]. Hole mobility is comparable to literature data [17, 18, 20].

Mobility model and validation
The transport analysis is focussed on the lateral (110)/(110) interfaces of the FinFETs simulated as double-gate devices. For a fin height of 65nm this assumption is appropriate for fin widths below approximately 20nm. The \( n \)-type devices were simulated with the Multi Subband Monte Carlo (MSMC) approach that accounts for the subband quantization and for the
most important scattering mechanisms [22]. Fig.8 shows a sketch of the $\Delta_4$ and the $\Delta_2$ valleys in a (110)/[1T0] electron inversion layer. In unstrained devices the $\Delta_4$ valleys are the lowest due the largest quantization mass $m_{\text{qZ}}=0.315m_0$. It has been argued that, due to the non parabolicity of the $\Delta$ silicon valleys in the [110] direction, the parabolic effective mass approximation (EMA) is inaccurate for the $\Delta_2$ valleys yield good agreement of the EMA and the LCBB results [26]. Hole mobility was calculated starting from the band-structure obtained with a self-consistent $k\cdot p$ solver coupled to the Poisson equation (as in [6, 7]), and then by using the momentum relaxation time approximation and accounting for phonons and surface roughness scattering by following [6]. All the scattering rates were calculated using, for each subband, the envelope wave-function corresponding to $k=0$ [6]. The scattering parameters of Tab.1 were used for all the simulations of this paper. Figs.9 and 10 show good agreement with compressive $T_{\text{HH}}$, while a compressive $T_{\text{HH}}$ increases the hole mobility. Fig.20 shows that the $T_{\text{IW}}$ is not as effective as the $T_{\text{HH}}$ for device optimization. Fig.19 and Fig.20 show that the piezo-resistive model results in quantitative and even qualitative discrepancies w.r.t. the numerical simulations and underlines the need for a rigorous modeling approach.

Finally, the additive effect of different strain components is experimentally confirmed by the stress induced $I_{DS}$ improvements reported in Fig.21 for nano-scale FinFETs.

**Conclusions**

In summary, direct strain measurements, mobility characterization and physics-based modeling were used to explain and optimize strain in both n- and p-type FinFETs. Our results assessed and explained the potentials for large electron mobility enhancements produced by the vertical strain and discussed the impact of all the main strain components on the electrical mobility. All the main simulation predictions were confirmed by experiments.

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**References**

This work, 

very low channel doping concentrations below 

or FinFETs [18]. All devices have compared to literature data for planar MOSFETs at 300K for the (Fig.1).


Figure 1: Schematic of a FinFET indicating the stress components in the fin height $T_{1H}$, width $T_{1W}$ and length $T_{1L}$ direction in the Device Coordinate System (DCS). Complex stress configurations comprising several $T_{1H}$, $T_{1W}$ and $T_{1L}$ components may occur in the device. Also shown is the silicon Crystal Coordinate System (CCS).


Figure 3: Direct measurement by holographic interferometry of deformation in vertical direction, $\varepsilon_{zz}$, calculated from (004) fringes for 20nm wide fins (as pictured in Fig.2).


Figure 6: Measured electron and hole mobility at 300K for the $n$- and $p$-FinFETs of this work, compared to literature data for planar MOSFETs [17, 19, 20] or FinFETs [18]. All devices have very low channel doping concentrations below $5\times10^{15}$ cm$^{-3}$.


Figure 5: Maximum vertical strain $\varepsilon_{zz}$ in Si fin (a) post-TiN deposition and (b) after thermal cycle. As-deposited strain is due to intrinsic stress in TiN and, for post-thermal cycle, to plastic relaxation at high temperature. CTE is the coefficient of thermal expansion and E is Young’s modulus. $W_{fin}=16$nm and $T_{V2N}=7$nm.


Figure 2: Cross-section TEM image through the gate-plane of FinFETs with $W_{fin}=20$nm.


Figure 7: Measured electron and hole mobility at 77K for the $n$- and $p$-FinFETs of this work, compared to literature data for planar MOSFETs [19]. All devices have very low channel doping concentrations below $5\times10^{15}$ cm$^{-3}$.


Table 1: Scattering parameters used in all simulations. Electron optical phonons model from [23]. Screening is not accounted for in the hole mobility calculations, hence the $L_e$ is relatively large to reproduce the measured mobility vs. $F_{eff}$ slope at large $F_{eff}$ (see Fig.10).


Figure 4: Deformation in (a) lateral ($W_{fin}$) and (b) vertical ($H_{fin}$) directions, calculated respectively from (111) and (TT1) holographic fringes for 10nm wide fins.


Figure 9: Simulated and experimental electron mobility (unstrained) versus effective field in (110) inversion layers, at 300K and 133K. Measurements from [19].


Figure 10: Simulated and experimental hole mobility (unstrained): (a) versus the effective field $F_{eff}$ in (001) Si (for different temperatures); (b) versus the inversion density in (110) Si. Measurements from [21] (a), [17] (b).


Figure 8: $\Delta_1$ and $\Delta_2$ valleys for the electrons in a (110)/[100] Si inversion layer. Mobility enhancements are obtained when stress forces the re-population of the $\Delta_2$ valleys with the lowest mass $m_s$ in the transport direction (see Fig.1). $m_s$ is the quantization mass that enters the Schrodinger equation.
Figure 11: Hole equi-energy contour plots for the lowest subband at 100meV from the subband minimum for unstrained or strained (110) inversion layer.

Figure 12: Simulations and measurements [24] of electron mobility variations in uniaxially strained (110)/(110) bulk planar n-MOSFets.

Figure 13: Simulations and measurements [17] of hole mobility variations in uniaxially strained (110)/(110) bulk planar p-MOSFets.

Figure 14: Simulated stress induced electron mobility variations vs. $T_H$, $T_L$, $T_{IV}$ at $N_{inv}=8 \times 10^{12}$ cm$^{-2}$ in (110) Si. Results are also shown for the piezo-resistive model with the bulk Si coefficients [28].

Figure 15: Simulated stress induced hole mobility variations vs. $T_H$, $T_L$, $T_{IV}$ at $N_{inv}=8 \times 10^{12}$ cm$^{-2}$ in (110) Si. Results are also shown for piezo-resistive model with the bulk Si coefficients [28].

Figure 16: Measured and simulated electron mobility in n-FinFETs at 300K and 77K. Strain values $\varepsilon_xx=-0.8\%$ and $\varepsilon_yy=+0.3\%$ taken from Figs.4.

Figure 17: Measured and simulated hole mobility in p-FinFETs at 300K and 77K. Strain values $\varepsilon_xx=-0.8\%$ and $\varepsilon_yy=+0.3\%$ taken from Figs.4.

Figure 18: Simulated re-population of the $\Delta_2$ valleys in (110)/[110] n-FinFET vs. compressive $T_H$ (bottom x-axis). The top x-axis shows the stress induced $\Delta_2$ to $\Delta_1$ valley splitting that concurs with the quantization to the overall subbands splitting.

Table 2: Table summarizing the impact of different stress components on the electron and hole (110)/[110] FinFETs mobility.

Figure 21: Influence of additional uniaxial $\varepsilon_{xx}$ strain upon $I_{D,Sat}$ in FinFETs. Strain induced by epic-Si$_3$N$_4$-Ge$_x$ S/D for p-MOS and by wafer bending for n-MOS. $I_{D,Sat}$ is boosted by 13% for p-MOS with $x=25\%$ and by 21% for n-MOS with 460MPa stress. Uniaxial strain boosters are thus effective in presence of large $\varepsilon_{xx}$. 

Figure 20: Simulated stress induced electron and hole percentage mobility variations w.r.t. the unstrained case vs. $T_{IV}$ and for $T_H=1$GPa.

Figure 19: Simulated stress induced electron and hole mobility (a), and corresponding percentage mobility variations w.r.t. the unstrained case (b) vs. $T_L$, and for $T_H=1$GPa.

Figure 10: (a) Measured and simulated electron mobility in n-MOSFETs at 110nm/110nm with 460MPa stress. Uniaxial strain boosters are thus effective in presence of large $\varepsilon_{xx}$. 

Figure 13: Simulations and measurements [17] of hole mobility variations in uniaxially strained (110)/(110) bulk planar p-MOSFets.