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EDITORIAL

The SINANO Network of Excellence has contributed during the last three years to the building of a European research area in the field of nanoelectronics. This strong structuring between 44 partners all around Europe has become a key player at the European level. The SINANO network and partners have been deeply involved in the management, domain teams and working groups of ENIAC, the European Technology Platform for nanoelectronics.

The SINANO joint projects and facilities have led to major scientific results, proofs of the high level of research in Europe. Driven by the European scientific community, they are devoted to long term research and are complementary to the medium term projects led by the industry. They allow speeding up technological innovation and preparing the path for future industrial applications.

SINANO has developed strong links with the European industry and with other research laboratories and institutes in the United States and Asia. It has also supported many dissemination activities such as workshops, summer schools and conferences, contributing to the spreading of the excellence of research in Europe.

This second issue of the SINANO newsletter presents some of the results of the network during the last months.

Although the first funding phase, supported by the European Commission under the 6th Framework Program, comes to an end, the impetus that has been initiated will be now pursued. New structures will be implemented in order to go on with the objective of making Europe a leader in the research in nanoelectronics in the next decades.

SCIENTIFIC HIGHLIGHTS

In SINANO, many new materials and innovating architectures are studied for Si-based CMOS and beyond-CMOS nanodevice integration. A strong effort is also devoted to the

understanding and modelling of the physical and electrical properties of these nanoscale structures.

New channel materials for ultimate CMOS

Strained silicon on insulator wafers with a diameter of 200 mm successfully fabricated using thin relaxed SiGe buffer layers and wafer bonding (Forschungszentrum Jülich and IMEC)

Strained silicon (sSi) on insulator (SSOI) wafers with a diameter of 200 mm were successfully fabricated using thin relaxed SiGe buffer layers and wafer bonding. A unique approach was employed to relax the 180 nm thick SiGe layers. The so called “Juelich process” involves He ion

implantation and annealing for efficient strain relaxation during annealing. Overgrowth with a 200 nm strain-adjusted SiGe layer with a Ge content of 16at% at a substrate temperature of 690°C reduced the threading density.

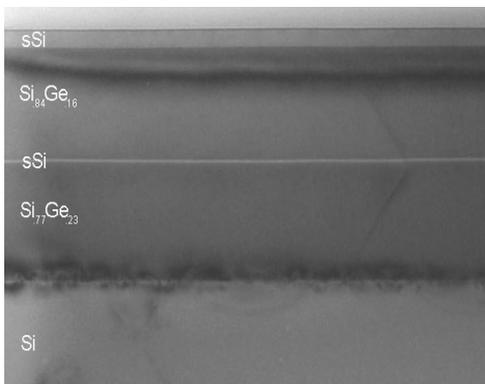


Figure 1 - XTEM image of a strain relaxed Si.77Ge.23 layer overgrown with a strain compensated 200 nm SiGe layer of 16at% Ge. The strained Si cap layer has a thickness of 40 nm.

Strained silicon on insulator wafers were produced by wafer bonding and hydrogen induced wafer splitting. The strain of the layers was measured by Raman spectroscopy revealing a strain of 0.66% in the tensile strained

Si after wafer bonding. The IR-image confirms perfect bonding. The corresponding cross-section TEM image shows a smooth 18 nm thick strained Si layer on top of a 100 nm BOX. The inset shows the perfect epitaxy of the sSi layer.

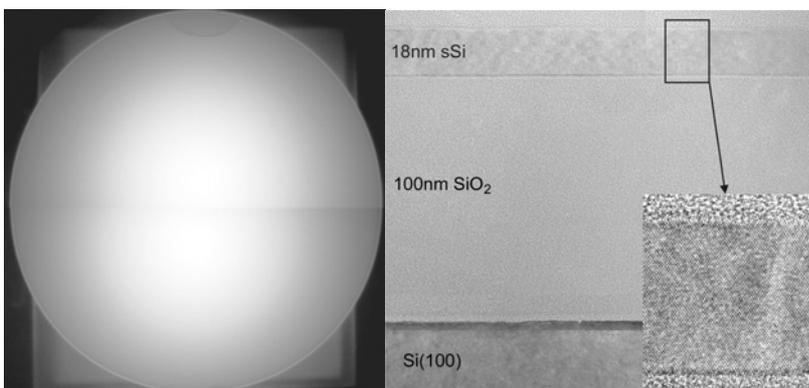


Figure 2 - Left side shows an infrared transmission image of a 200 mm sSi/SiGe wafer bonded to Si using a PE-CVD Oxide as a bonding layer. The right XTEM image of an SSOI wafer shows 18 nm strained Si on 100 nm SiO2 after wafer bonding. The inset shows a magnification of the single crystalline sSi layer.

Highly-strained silicon structures developed (Stuttgart University, Newcastle University and KTH)

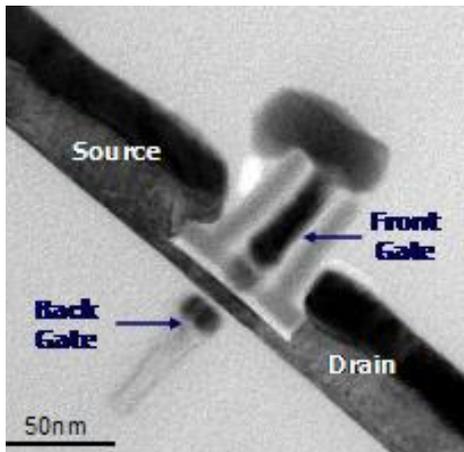
Structures of highly-strained Si with smooth surface morphology (rms ~ 0.2nm) on ultrathin near 100% relaxed virtual substrates with 20%Ge content are developed, grown by molecular beam epitaxy with in situ growth

monitoring and investigated ex situ. Electron mobility enhanced by 67% in strained-Si channels (compared to control Si devices) is observed at effective electric field of 1.2MV/cm.

Non-classical nano-MOSFET architectures

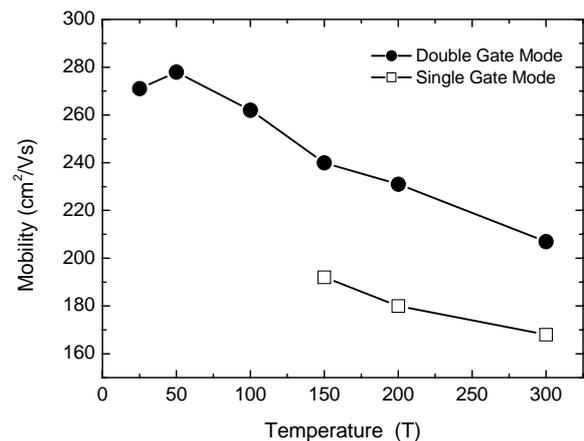
Experimental evidence of mobility enhancement in short-channel ultra-thin body double-gate MOSFETs (CNRS-IMEP and CEA-LETI)

This work shows for the first time an experimental evidence of mobility enhancement in ultra-thin body double-Gate (DG) MOSFETs using magnetoresistance mobility extraction technique. The results show a clear mobility



TEM cross-section of the devices tested

improvement in double-gate mode compared to single-gate mode mobility at the same inversion charge density. This is explained by the role of volume inversion in ultra-thin body transistor operating in DG mode.



Variation of maximum magnetoresistance mobility with temperature for single gate (squares) and double gate mode (circles)

FinFETs perspectives for analog and RF applications in a wide frequency range analyzed through measurements and 3D simulations (UCL and IMEC)

We have analyzed FinFETs perspectives for analog and RF applications in a wide frequency range (from DC up to 500 GHz) through measurements and 3D simulations. The volume inversion regime was demonstrated to be beneficial yielding increased Early voltage, drive current and transconductance, which further translates in higher achievable cut-off frequency and intrinsic gain even in the sub-50nm devices. In addition, high (nearly ideal) transconductance-to-drain current ratio are achieved in multi-gate devices thanks to their better control of short-channel effects, which makes them also promising for the baseband applications. But in the same time multi-gate

devices suffer from the enhanced parasitic capacitances related to their more complex 3-D interconnections of the gate, source, and drain contacts. It was shown that an increase of W/L ratio leads to a decrease of the normalized parasitic capacitance, proving that the important part of this capacitance is related to the fringing fields from gate-to-source and to drain through the buried oxide. Therefore, the increase of fin height will contribute to the decrease of the relative importance of parasitic capacitances related to their 3-D structure, and then the possibility to reach higher RF performance, as well as higher drive current per unit die area.

Extensive study of the effective mobility in FinFET structures using a dedicated split C-V technique performed (ISP Kiev, UCL and IMEC)

An extensive study of the effective mobility in FinFET structures has been performed, using a dedicated split C-V technique. In the case of doped-channel devices, a strong enhancement of hole mobility, and also surprisingly of electron mobility has been found at low and moderate inversion charge densities in narrow FinFETs, in which fin sides with the (110) surface orientation

dominate, as compared to their counterpart very wide-fin (quasi-planar) devices, in which the top channel with (100) orientation is prevailing. This surprising enhancement of electron mobility in narrow FinFETs was attributed to lower doping of fin sidewalls compared to the top channel resulting in lower Coulomb scattering, and FD DG-type operation of narrow-fin devices

resulting in a lower electric field and a deeper inversion charge centroid. Similarly, these factors contribute to the improvement of hole mobility in doped-channel narrow FinFETs, along with improvement due to the (110) fin surface orientation. The effect of the fin width on the effective mobility in FinFETs with an

undoped channel has been studied as well. It has been found that the electron mobility in FinFETs is nearly invariant with the fin width, while hole mobility noticeably increases with decreasing fin width from 55 nm to 25 nm, that could be attributed to the effect of the fin surface orientation.

New method for the fabrication of planar Double-Gate (DG) MOS devices investigated (UCL and Chalmers University of Technology)

A novel method for the fabrication of planar Double-Gate (DG) MOS devices has been investigated at UCL. Successfully fabricated Single-gate (SG) and DG MOSFET devices on the same wafer have been fully characterized and their electrical performances compared. The planar DG devices were fabricated using wafer bonding over pre-patterned cavities. The wafer

bonding conditions (surface activation and annealing conditions) were optimized to transfer properly a high quality thin silicon layer from a SOI wafer onto a pre-etched cavity in an oxidized bulk silicon wafer. Preliminary electrical characterization results show that the built planar DG devices exhibit the expected theoretical performances.

Emerging silicon-based logic and memory nanodevices

Worldwide first step-and-repeat nanoimprint lithography system for industrial fabrication of nanoscale devices installed in Germany

AMO GmbH, a partner of the SINANO network based in Aachen, Germany, has developed, manufactured and installed an automated step & repeat UVbased Nanoimprint Lithography (UV-NIL) system, the EVG770 NILStepper.

This private non-profit company is committed to applied research in the area of micro-, nano- and optoelectronics. The department AMICA (Advanced Microelectronic Center Aachen) is dedicated to nano lithography technology with major emphasis on UV-NIL activities.

UV-NIL is a next-generation lithography technology technique and a potential contender to succeed optical lithography for the 32-nm node, according to the International Technology Roadmap of Semiconductor (ITRS).

AMO is working on UV-NIL for performing R&D and small scale production for applications in the

area of photonic devices, nanoelectronics, and life sciences. Nanoimprint lithography is an innovative patterning technology that provides a lower cost-of-ownership model compared to current manufacturing lithography tools.

The step-and-repeat NIL system offers a lithography resolution down to 10 nm and targets sub-50-nm overlay alignment accuracy via a novel dual-stage alignment approach.

This new equipment results from a joint development program with EVGroup. Based in Austria, EV Group is a leader in lithography for advanced packaging and nanotechnology. It has the largest installation base worldwide for single-step imprinting equipment and this new NIL stepper enhances the company's product portfolio substantially.

Feasibility of Si nanowire integration: CVD growth, characterization, and comparison of Au vs PtSi catalysts (FMNT and CEA Grenoble)

Silicon nanowires (Si NWs) are promising materials for some of the basic building blocks in microelectronics (interconnects, transistor channels, nanoelectrodes, etc.) and emerging application areas of photonics, chemical sensing, and solar cells. We have studied the growth of Si NWs combining a metal catalyzer and CVD processing with silane precursor gas. TEM and EDX experiments clearly show the presence of Au, used as catalyst in the VLS

method, at the sidewalls of NWs. Because Au is not CMOS-compatible, several other microelectronics-friendly metals are studied. In particular, we show that PtSi can be used as an efficient solid catalyst with particles size varying between 20 nm and 100 nm. For the PtSi case, NW growth proceeds via solid-phase epitaxy which differs significantly from the traditional vapor-liquid-solid process using Au.

Reliable single-electron-transistor made from modulation of doping in SOI nanowires (CEA-LETI and CEA-DRFMC)

A simple and highly reproducible single electron transistor (SET) has been fabricated using gated silicon nanowires. The structure is a metal-oxide-semiconductor field-effect transistor made on silicon-on-insulator (SOI) thin films. The channel of the transistor is the Coulomb island at low temperature. Two silicon nitride spacers

deposited on each side of the gate produce a modulation of doping along the nanowire that creates tunnel barriers. The period of the Coulomb oscillations is set by the gate capacitance of the transistor and therefore fully controlled by lithography.

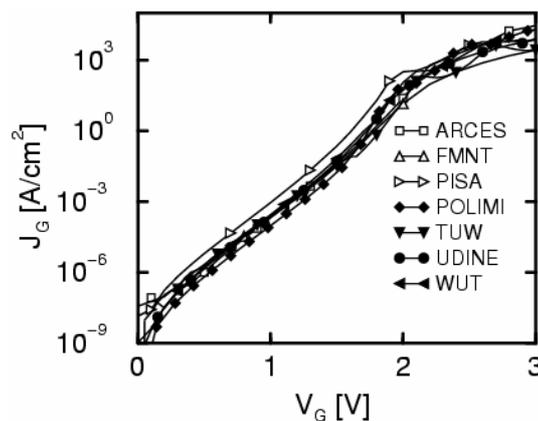
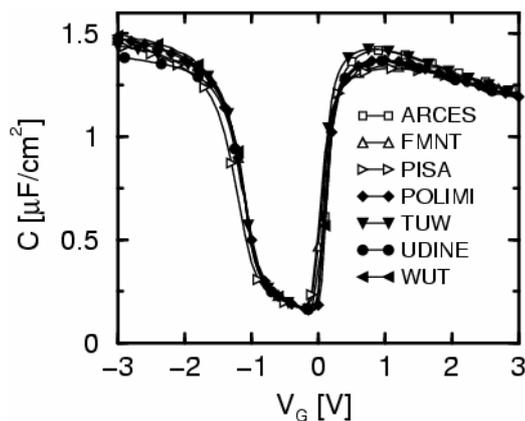
Modelling and Simulation of nanodevices

Comparison between models for gate current computation (Arces, FMNT, Pisa University, Politecnico di Milano, Wien Technical University, Udine University, Warsaw Technical University, Birmingham University)

One of the main activities of this workpackage is the benchmarking of the different models and modeling tools developed by the SINANO partners. We have compared the results of various models for the capacitance/voltage and leakage current estimation in advanced gate-stacks. This has been an unprecedented collaboration between Nanoelectronics research groups in Europe.

The comparison between the different models has been carried out on template gate-stacks, including pure silicon-dioxide dielectrics as well as stacks featuring high-k materials. To make the comparison more efficient, all groups have

been forced to use the same model parameters. The modeling approaches used by the partners include solutions of the Schrödinger equation with open as well as closed boundaries, and different approaches to compute the tunneling probability and the escape-time from the bound states in the inversion layer. In spite of these modeling differences, good agreement between results has been found for all the template devices. As an example, the figures show the simulated capacitance/voltage and the current/voltage characteristics for a gate-stack featuring 4nm of HfO₂ and a SiO₂ interfacial layer of 1nm.



Modeling quasi-ballistic transport in nano-MOSFETs (CNRS-IMEP, Udine University)

With the amazing progress of silicon technology, typical dimensions of electronic devices are so small that Physics is drastically changing. One of the most striking examples is the so-called “ballistic transport”, which means that electrons can move from one side of the devices to the other, without suffering any scattering event. While this regime of transport does not really occur in current devices, it has been demonstrated that they can operate close to it,

opening new perspectives for technological device optimization.

We are tightly cooperating on this task, and are investigating the validity of the models for back-scattering, both analytically and by using the Multi-Subband Monte-Carlo device simulators. In particular the two formulas proposed by the Purdue’s group for r have been considered:

$$r_{LF} = \frac{L}{L + \lambda} \quad \text{in the low-field limit, and}$$

$$r_{HF} = \frac{L_{kT}}{L_{kT} + \lambda}$$

is the extension of the kT-layer. Fig.1 shows that if we use the mean-free-path λ as a fitting parameter, the analytical formula reproduces quite well the Monte-Carlo simulations. Our analytical studies have shown that these formulas can be derived from the Boltzmann-

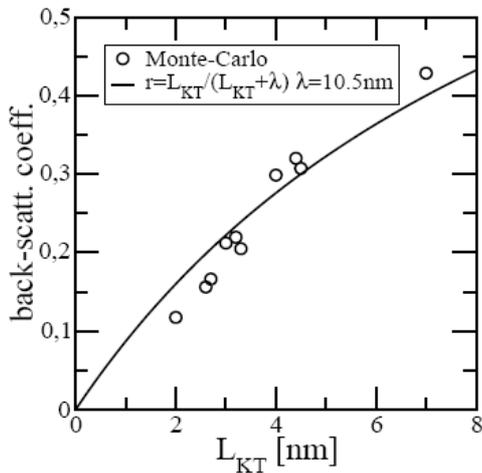


Figure 1

Transport-Equation by assuming a “relaxation-length” approximation for the collision term. Furthermore, we could demonstrate that the formula for high-fields requires the back-scattered carrier flux to be a thermalized Maxwellian. The same analysis has provided a new equation that links the low and high field limits (Fig.2).

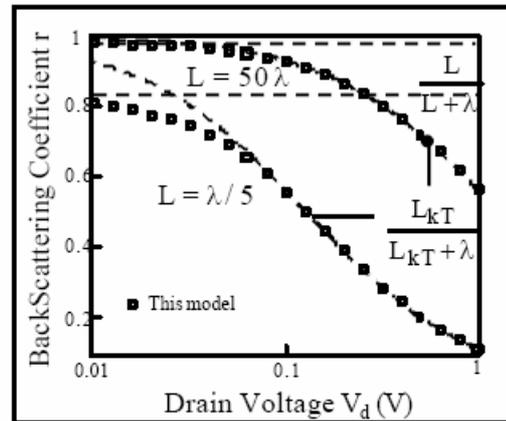


Figure 2

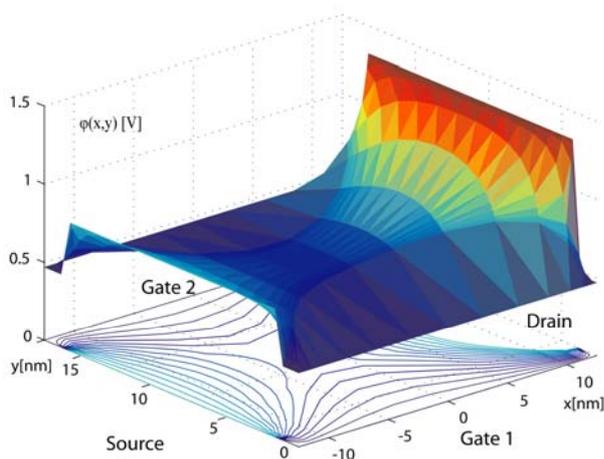
A new framework for compact modeling of nanoscale MOSFETs (URV, UNIK)

Nanoscale double gate (DG) and cylindrical gate-all-around (GAA) MOSFETs are primary candidates for replacing the conventional bulk MOSFET in the coming five to ten years, to meet the ever growing demand for high-speed, low-power CMOS circuitry. Precise compact models for these devices are needed for implementation in circuit simulators and circuit design tools. To achieve the needed model accuracy, the higher-dimensionality of the potential and inversion charge distributions has to be taken into account.

A framework for such modeling has been developed. An essential part of this is a precise description of the device electrostatics of the

capacitive coupling between gate, source and drain electrodes bordering to the device body. Our models are based on the use of conformal mapping techniques, which allows a precise solution of the Laplace's equation for the DG body in the subthreshold regime, thus providing the channel barrier topography and its dependence on geometry, materials, and applied voltages. Hence, scaling and short-channel effects are automatically included in the formalism.

Excellent agreement on electrostatics and drain current has been found between the model and numerical simulations.



Modeled subthreshold potential distribution for DG MOSFET with applied drain bias

TRAINING ACTIVITIES

The training of researchers and students from partners of the network or outside is an important task of SINANO. More than a hundred weeks of exchange and training are realized each year between the different partners.

Many SINANO members are also involved in the organization of summer schools. Thus, SINANO

supports each year the International summer school on advanced microelectronics (MIGAS) and the European school on nanoscience/nanotechnology (ESONN) that are organized by the CNRS and the CEA in Grenoble and its surroundings.

Successful 2nd edition of the SINANO Modeling School

The SINANO Summer School on Device Modeling and Simulation aims to provide an opportunity for the dissemination and the discussion of the results obtained by academic and industrial research groups involved in the physics, modeling and characterization of advanced silicon-based devices. The first edition of the School was held in Glasgow in August 2005.

The interest raised showed the relevance of this event and a second edition was therefore organized in August 2006 by the ARCES Research Center of the University of Bologna. It was held at the University Residential Center in Bertinoro, Italy.

The program included four sessions, each comprising lectures from outstanding invited speakers from Japan, USA and Europe.

The first day has been devoted to an introduction to advanced physical models for Device and Process Simulation.

The second and third were dedicated to the analysis of advanced techniques for device-simulation and to the description of relevant case-studies involving nano-scale devices.

The fourth day was devoted to analytical and compact models for device and circuit analysis and design.

During the fifth day, lectures covered advanced experimental characterization techniques and the integration of device and process simulation for advanced Technology-CAD.

Two comprehensive laboratory sessions introduced to Monte Carlo simulation and to quantum-mechanical modeling of MOS devices.

The school has been attended by more than sixty students from Europe and Asia.

DISSEMINATION

2nd edition of the SINANO workshop at the ESSDERC-ESSCIRC conference

The ESSDERC-ESSCIRC Conference, the major event in Europe in the field of solid-state devices, technologies and circuits, hosted for the second time a SINANO Workshop in September 2006. The aim of this Workshop was to present the status and trends of CMOS and beyond-CMOS nanodevices for terascale Integrated Circuits. The following talks have been given during this day that gathered more than a hundred people.

- "New generation of SiGe virtual substrates" - T. Grasby, Warwick University
- "Strain characterisation in advanced Si devices" - S. Olsen, Newcastle University

- "Characterization of Nanoscale dielectrics" - O. Engstrom, M. Lemme, P. Hurley, S. Hall, Chalmers Univ., AMO, Tyndall, Liverpool University
- "Reliability degradation characteristics of ultra-thin gate dielectrics for Nano-CMOS application" - J.F. Kang et al, Beijing University
- "Comparison among modelling approaches for gate current computation in advanced gate stacks" - P. Palestri et al, University of Udine
- "Comparison among modeling approaches for drain current computation in nanoMOSFETs" - C. Fiegna et al, University of Bologna

- "CMOS for next 15 years as the mainstream of nano device technology: problems, solutions and beyond that" - H. Iwai, Tokyo Institute of Technology
- "Emerging devices for enhancing and beyond the CMOS technology" - W.-X. Ni, National Nanodevice Laboratories, Hsinchu
- "Quantum transport in semi-conductor nanowire MOSFETs: influence of the bandstructure" - M. Bescond, IMEP-CNRS
- "Silicon Nanodots and related structures for memory application" - A.G. Nassiopoulou, A. Salonidou, O. Winkler, B. Spangenberg, H. Kurz, A. Souifi, V. Bayot, A. Nazarov, IMEL, RWTH, LPM-CNRS, UCL, SPI
- "Ultimate CMOS-compatible tunneling devices" - A. Zaslavsky, Brown University

All presentations can be downloaded on the SINANO website:
<http://www.sinano.org/index/public/17/workshop2006.html>

Other events

These other events held during 2006 have been supported by SINANO. More information about them can be found on the SINANO website (<http://www.sinano.org/index/public/17/95.html>).

- **7th European Workshop on ULtimate Integration of Silicon (ULIS)**, Grenoble, France, 20-21 April 2006 (organized by CEA and CNRS)
- **Workshop on Nanoelectronics and Photonics Systems (NEPHOS)**, Tarragona, Spain, 26 - 27 June 2006 (organized by Universitat Rovira i Virgili)
- **Symposium on “Silicon Nanocrystals for Electronics and Sensing Applications” and symposium on “Germanium based semiconductors... from materials to devices”**, Nice, France, (during the E-MRS spring meeting), 29 May-2 June 2006 (organized by IMEL and IMEC)
- **7th Symposium "Diagnostics & Yield: Advanced Silicon Devices and Technologies for ULSI era"**, Warsaw, Poland, 26-28 June 2006 (organized by Warsaw Technical University)
- **International SINANO Workshop on “Epitaxy for Si nanoelectronics”**, Aix-en-Provence, France, 6-7 July 2006 (organized by the University of Stuttgart)
- **Nanoelectronics Days**, Aachen, Germany, 11-13 October 2006 (organized by Forschungszentrum Jülich)
- **Workshop on Nanoscaled semiconductor-on-insulator structures and devices**, Sudak, Ukraine, 15-19 October 2006 (organized by the Institute of Semiconductor Physics in Kiev)
- **Workshop on Silicon Nanodevices “Beyond CMOS: Emerging Nanodevices”**, Aachen, Germany, 7-8 November 2006 (organized by RWTH)

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