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# Influence of regrowth conditions on the hole mobility in strained Ge heterostructures produced by hybrid epitaxy

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Strained Ge *p*-channel heterostructures have been produced using a hybrid-epitaxy method, which allows the advantages offered by different growth techniques to be exploited. Chemical vapor deposition of thick strain-tuned virtual substrates has been combined with growth of the active layers by solid-source molecular beam epitaxy. This paper discusses optimization of the regrowth conditions, to achieve a high hole mobility, and correlates structural characterization with electrical measurements. Initial *ex situ* chemical cleaning of the virtual substrate was found to be essential for successful regrowth. Structural analysis, using cross-sectional transmission electron microscopy and atomic force microscopy, showed that the regrowth temperature significantly affects the growth mode of the active layers and that planar growth was only achieved below 400 °C. Samples with Ge channels from 8 to 30 nm thick were analyzed with plan view transmission electron microscopy to study the formation of misfit dislocations and estimate the degree of relaxation—two effects detrimental to hole transport properties. For intermediate thickness layers, postgrowth annealing at 650 °C was found to significantly improve the hole mobility, by eliminating point defects but not leading to substantial relaxation. As a result, the mobility was found to almost double at room temperature and increase fourfold at 10 K. The level of diffusion and interface integrity, for both the as-grown and annealed structures, has been investigated using low energy secondary ion mass spectrometry. © 2004 American Institute of Physics. [DOI: 10.1063/1.1811784]

## I. INTRODUCTION

The Si semiconductor market has been following a trend where the speed of Si devices has doubled every 18 months. This exponential trend was observed back in 1965 by Gordon Moore and, commonly known as “Moore’s Law,”<sup>1</sup> is now enshrined within the International Technology Roadmap for Semiconductors. Such device speed enhancements have, until recently, been achieved by means of aggressive device scaling but the limitations associated with modern lithographical processes and the thermal problems associated with smaller devices are now becoming limiting factors. A secondary issue is that, in the case of conventional Si complementary metal oxide semiconductors (CMOS), *n*-MOS devices have a higher mobility than the *p*-MOS devices, leading to a significant difference in device size and affecting both current drive parity and threshold voltage symmetry.<sup>2</sup> Research has therefore turned to other solutions in order to try and continue the Moore’s law trend. One such solution is the incorporation of Ge into Si based technology, since bulk Ge exhibits a much higher mobility for both electrons and holes compared to Si.<sup>3</sup> However, Ge has for a long time been ignored for MOS devices due to processing difficulties and especially the lack of a high quality gate dielectric comparable to SiO<sub>2</sub>. Now dielectric materials with a permittivity much greater than SiO<sub>2</sub> are being developed for aggressively scaled Si devices and, since they can be directly deposited, these so-called “high *K*” dielectrics should enable Ge to become more readily integrated within the CMOS ap-

plication field. Research is particularly concentrating on the large hole mobility enhancements offered by strained Ge, which would bring more parity between *n*- and *p*-MOS devices.

Given the difference in lattice constant between Si and Ge (~4.2%) and their total miscibility, a sufficiently thin layer of epitaxially grown Si<sub>1-x</sub>Ge<sub>x</sub>, or pure Ge, may be forced to elastically distort and take on the in-plane lattice spacing of the Si substrate. In order to accommodate such a distortion the layer stretches perpendicular to the substrate and is referred to as being under compressive biaxial strain. Such strain has a profound effect on the valence band, distorting and splitting the heavy- and light-hole bands, which leads to a reduced effective mass and increased carrier relaxation time,<sup>4</sup> both of which increase the hole mobility. Previous work on the incorporation of Ge into Si includes pseudomorphic Si<sub>1-x</sub>Ge<sub>x</sub> layers (*x* ≤ 0.5) grown on Si substrates. Hall hole mobilities of 150 cm<sup>2</sup>/V s at 300 K and 2500–9300 cm<sup>2</sup>/V s at 4.2 K for such types of structures have been obtained.<sup>5,6</sup> It has been predicted, from calculations where phonon scattering is the dominant mechanism and interfaces are ignored, that a higher hole mobility at room temperature (RT) would be obtained for a structure containing a pure Ge channel.<sup>7</sup> To grow a strained Ge channel directly on Si without it relaxing, the Ge layer could be no more than 1 nm thick, which is too thin for effective carrier confinement. In order to produce a thicker Ge channel (up to tens of nanometers), the Ge layer must be grown on a Si<sub>1-y</sub>Ge<sub>y</sub> virtual substrate (VS). The terminating Ge content of the VS is chosen to be in the range *y* = 0.6–0.7, since this

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gives the same level of strain within the Ge channel as found in strained pseudomorphic  $\text{Si}_{1-x}\text{Ge}_x$  layers with  $x=0.3-0.4$  that yield the best hole mobility. In this way, Ge  $p$ -channel Hall mobilities in the range  $1300-2100 \text{ cm}^2/\text{V s}$  at 300 K (Refs. 8 and 9) and  $55\,000-120\,000 \text{ cm}^2/\text{V s}$  at 4.2 K (Refs. 10 and 11) have previously been demonstrated.

In this paper, we present Ge channel heterostructures grown by a method of hybrid epitaxy. Hybrid epitaxy gives the flexibility to take advantage of the strengths offered by various epitaxial growth technologies. In this work the thicker layers of the virtual substrate were produced rapidly using ultrahigh vacuum chemical vapor deposition (UHV-CVD) while the thinner, active layers were grown by solid source molecular beam epitaxy (SS-MBE) at lower temperatures. The structures grown had excellent hole transport properties<sup>12</sup> and, in this paper, we report on the structural aspects associated with achieving such good quality transport. The techniques employed are cross-sectional transmission electron microscopy (XTEM), plan view TEM, atomic force microscopy (AFM), and low energy secondary ion mass spectrometry (SIMS). From analyzing the results we discuss growth limiting factors, the effects of postanneal diffusion and relaxation from misfit dislocations.

## II. SAMPLE GROWTH

The starting substrates used were linearly graded  $\text{Si}_{1-y}\text{Ge}_y$  ( $y=0.6$ ) VSs grown by UHV-CVD at MIT. The graded region had been produced using a grading rate of 10% Ge per micron and was terminated with a  $1 \mu\text{m}$  constant compositional layer which should be fully relaxed.<sup>13</sup> Before the second phase of epitaxial growth, at Warwick, the wafers were cleaned *ex situ*. Typical *ex situ* chemical cleaning procedures used on Si substrates (RCA stages I and II) had been found to be highly reactive, with etch rates  $\sim 100$  times greater for layers containing 60% Ge than for pure Si. As such control is a problem and can easily lead to removal of the whole of the constant composition terminating layer and even some of the graded region. It is essential for successful regrowth that the terminating layer of the VS remains intact, relaxed and with a minimum number of dislocations that should be confined to the graded region, otherwise the substrate is rendered useless. The chemical cleaning procedure involved a 3 min Piranha etch ( $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ ) followed by a 2% HF dip before spinning dry. To grow the active Ge channel heterostructure, the cleaned VSs were then loaded into the Vacuum Generators V90s SS-MBE system and subjected to an *in situ* high temperature desorb for 30 min at  $860^\circ\text{C}$ , to drive off the hydrogen terminating the wafer surface. Following this the temperature was lowered and growth of the structure commenced. The regrowth structures consisted of a 200 nm lattice matched, constant-composition layer grown at  $800^\circ\text{C}$ , with a further 300 nm grown while the temperature was lowered to the required active layer growth temperature (in the range of  $350-500^\circ\text{C}$ ). Growth was interrupted for 30 min after this initial 500 nm of relaxed material, to ensure the wafer had stabilized at the lower growth temperature. Following this growth interrupt, a layer stack was grown consisting of 20 nm  $\text{Si}_{0.4}\text{Ge}_{0.6}$ , a 5 nm sup-

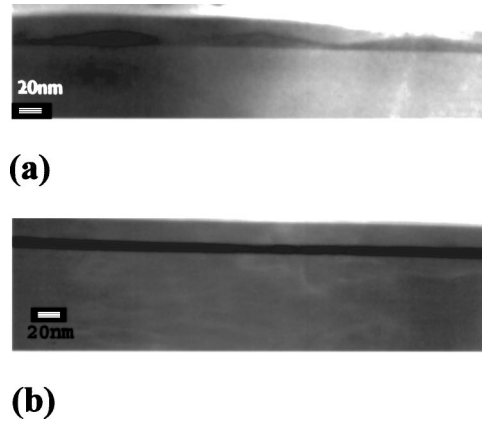


FIG. 1. XTEM images of 8 nm Ge channel structures grown (a) at  $490^\circ\text{C}$ , showing almost 3D growth, and (b) at  $350^\circ\text{C}$  where the Ge channel (dark band) appears smooth.

ply layer of  $\text{SiGe:B}$  (with a B doping level of  $3.6 \times 10^{18} \text{ cm}^{-3}$  measured by SIMS), a 15 nm undoped setback layer of  $\text{Si}_{0.4}\text{Ge}_{0.6}$ , the Ge channel (with thickness in the range 8–30 nm for different samples), a 20 nm  $\text{Si}_{0.4}\text{Ge}_{0.6}$  capping layer, and finally the structure was terminated with a 2 nm Si cap. Parameters that were varied in these experiments were the Ge channel thickness and the active layer growth temperature.

## III. EFFECTS OF REGROWTH TEMPERATURE

Several structures were initially grown with a 8 nm channel at a variety of growth temperatures between  $350$  and  $490^\circ\text{C}$ . All the structures were found to have a smooth lower interface to the channel but to incorporate a large amount of roughening at the upper channel interface, with layers grown at the highest temperatures ( $\geq 450^\circ\text{C}$ ) bordering on three-dimensional (3D) island growth as visible from the XTEM image in Fig. 1(a). Similar roughening has been observed before and attributed to the balance between the growth surface strain and surface step energies.<sup>14</sup> Figure 2(a) shows a  $1 \times 1 \mu\text{m}^2$  AFM image of a sample surface grown at  $490^\circ\text{C}$ , reaffirming the roughening observed by XTEM and clearly showing that it takes the form of faceting, an effect known to be associated with high growth temperature.<sup>15</sup> The islands produced are quite regularly arranged and are visible in Fig. 2(a) with a typical size of  $\sim 200 \text{ nm}$ . Even within the relatively smooth region of a single island there are strain fluctuations that show up in the diffraction contrast of the plan view TEM in Fig. 2(b).<sup>16</sup>

For all the structures regrown at temperatures below  $400^\circ\text{C}$ , Hall measurements performed on large Van der Pauw crosses showed similar mobilities at RT ( $750 \pm 100 \text{ cm}^2/\text{V s}$ ) and at 10 K ( $3000 \pm 100 \text{ cm}^2/\text{V s}$ ), and a hole density of  $\sim 2 \times 10^{12} \text{ cm}^{-2}$  irrespective of regrowth temperature. To understand these results, 1D Poisson/Schrödinger modeling of the intended 8 nm channel structure was performed and Fig. 3(a) shows the valence band and predicted carrier distribution within the Ge channel region. From the modeled carrier distribution it is observed that both interfaces of the Ge channel would have a strong influence on the confined carriers. Thus, to improve the mobility, the



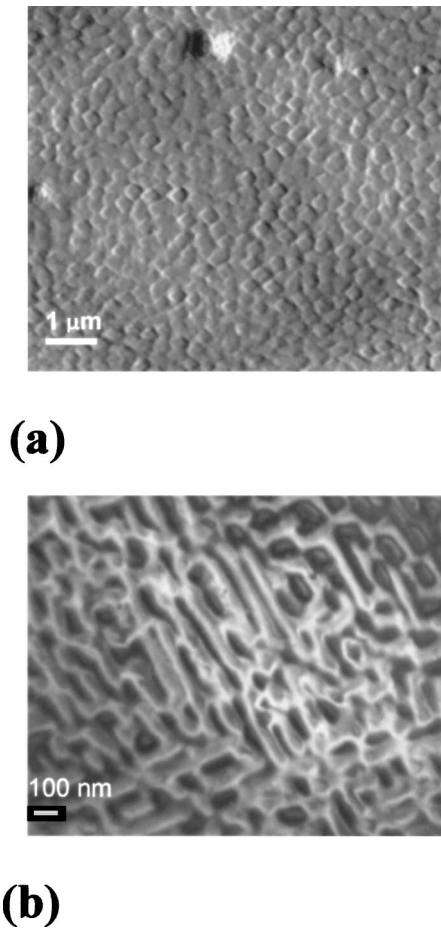


FIG. 2. Images of the 8 nm Ge channel structures grown at 490 °C. (a) AFM showing facet growth and  $\sim 200$  nm islands. (b) Plan view TEM of a single island showing strain fluctuations. Scale bars are (a) 1  $\mu\text{m}$  and (b) 0.1  $\mu\text{m}$ .

upper interface roughening must be suppressed by either removing the roughening or changing the layer structure so that carriers do not come into contact with this rough interface.

Roughening of the upper interface was finally suppressed when the growth temperature was lowered to 350 °C, as shown in the XTEM image of Fig. 1(b). The reduction in surface roughness as the growth temperature is lowered from 490 to 350 °C can be clearly seen in the AFM images of Fig. 4. Quantitative analysis of these images is complicated because microroughening on the 100 nm scale arising from regrowth, and thought to most affect the mobility, is superimposed on larger scale ( $\sim 1 \mu\text{m}$ ) undulations from the VS. To concentrate on the smaller scale, rms roughness values have been averaged from several  $250 \times 250 \text{ nm}^2$  windows in different regions of the image, giving values of 2.4, 1.0, and 0.4 nm for the structures grown at 490, 460, and 350 °C, respectively.

Hall measurements on the sample grown at 350 °C only yielded a small hole mobility improvement at RT (to  $920 \text{ cm}^2/\text{V s}$ ) compared with the previous structures grown above 400 °C, but the 10 K mobility was enhanced by more than a factor of 2–7300  $\text{cm}^2/\text{V s}$  without any significant change in carrier density. This makes it clear that the low

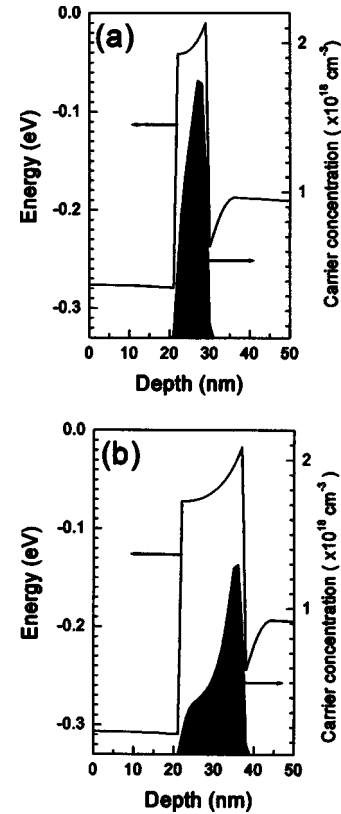


FIG. 3. 1D Poisson Schrödinger simulations of the valence band energy and hole density of the heterostructures with (a) 8 nm and (b) 16 nm channels. The valence band discontinuities mark the division between the Ge channel and  $\text{Si}_{0.4}\text{Ge}_{0.6}$  cladding layers. It can be seen that while both interfaces will influence carriers in the narrow well, the upper interface becomes less important as the channel thickness is increased.

temperature mobility was being significantly limited by scattering at the rough upper interface for the structures produced at higher temperature.

#### IV. EFFECTS OF GE CHANNEL THICKNESS

Further 1D Poisson/Schrödinger modeling of the inverted modulation doped structure indicated that by increasing the Ge channel thickness, the confined carriers would only be influenced by the lower interface [Fig. 3(b)]. A set of samples with varying Ge channel thickness (16, 20, and 30 nm) were grown at 350 °C.

Figure 5(a) shows a plan view TEM image of the 8 nm channel structure, with a small amount of surface morphology only being observed at the highest magnification and no sign of cross-hatch patterns. By contrast, the thicker samples were found to have misfit dislocations present, as can be seen in the plan view TEM micrograph from the 20 nm channel structure [Fig. 5(b)]. The formation of misfit dislocations implies the layers were strained in the early stages of growth, but as the layer thickness exceeded the equilibrium critical thickness plastic relaxation occurred. The extent of this plastic relaxation  $R$  was determined using the relation  $R = b_{\text{eff}}\rho_{\text{MD}}$ , where  $\rho_{\text{MD}}$  is the misfit dislocation line density and the effective Burgers vector  $b_{\text{eff}}$  is the component responsible for misfit strain relief.<sup>17</sup> For these structures, the misfit dislocations will be at  $60^\circ$  so  $b_{\text{eff}} = \alpha_{\text{Ge}}/2\sqrt{2}$  where  $\alpha_{\text{Ge}}$  is the

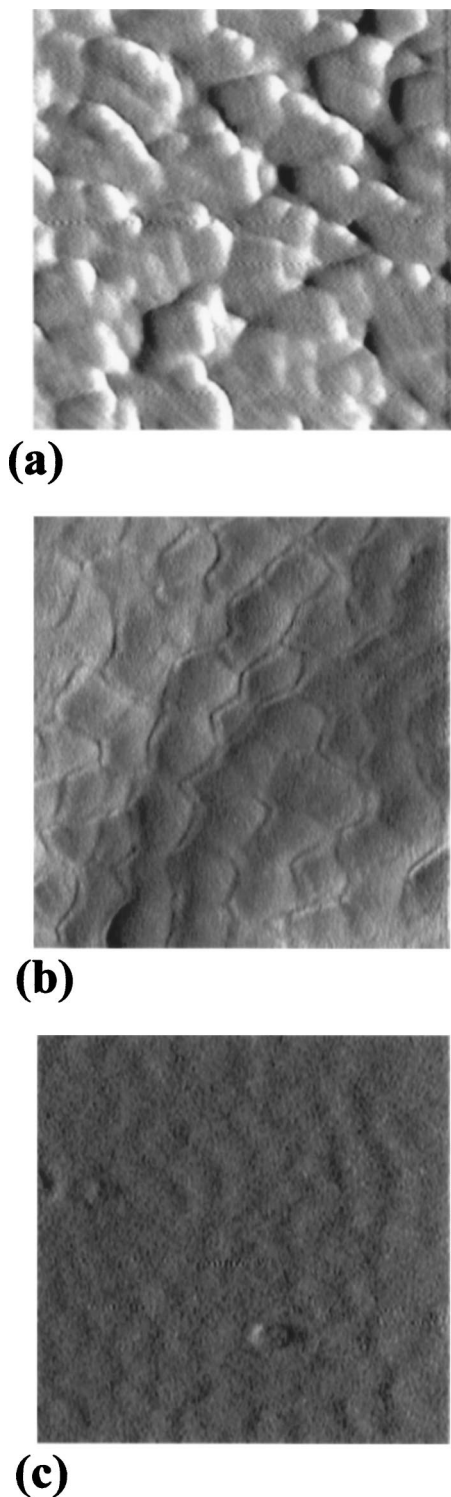


FIG. 4. AFM images of 8 nm Ge channel structures, showing the reduction in surface roughness as the growth temperature is lowered from (a) 490 °C through (b) 460 °C to (c) 350 °C. In each case the field of view is  $1 \times 1 \mu\text{m}^2$ .

germanium lattice constant ( $5.658 \text{ \AA}$ ). The observed dislocation density and plastic relaxation determined from this are given in Table II from which it can be seen that, while the 20 nm Ge channel remains fully strained, there has been significant relaxation for the 30 nm channel.

From Hall measurements, the RT and 10 K hole mobility for the thicker Ge channel structures were found to be only

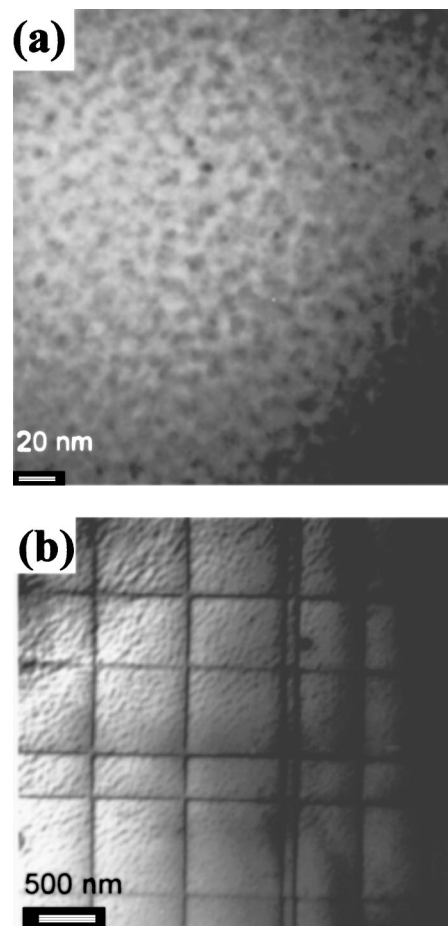


FIG. 5. Plan view TEM images of samples grown at 350 °C with Ge channels of (a) 8 nm and (b) 20 nm, showing the appearance of misfit dislocation in the thicker layers.

slightly improved on those of the 8 nm structure (see Table I). Such similarity suggests that the upper interface is no longer the factor most influencing carrier mobility for these low growth temperature samples. It also suggests that the misfit dislocations in the thicker layers are not limiting the mobility. However, the 10 K mobility is still much lower than other published data on Ge channels<sup>10,11</sup> so there must be another mechanism preventing the full potential of the layers from being realized.

## V. EFFECTS OF POSTGROWTH ANNEALING

It has previously been shown that high densities of point defects are present within pseudomorphic SiGe layers grown at low temperature and that by annealing this density can be reduced leading to much enhanced electrical properties.<sup>18</sup> Given the low growth temperature (350 °C) used to suppress roughening, it was extremely likely that point defects would be present, so the samples were annealed within the temperature range 600–700 °C for 30 min under dry  $\text{N}_2$ . To assess the electrical quality, Hall measurements were made between 10 K and RT. The largest mobility enhancement was found at 650 °C, as can clearly be seen in Fig. 6 for the 20 nm channel sample. Table I summarizes the RT and 10 K mobility, as a function of channel thickness, for the structures as-grown and following the optimal annealing conditions

TABLE I. Measured Hall mobility at 300 and 10 K from heterostructures with various Ge channel thickness, before and after annealing at 650 °C, together with the enhancement produced by annealing. The carrier density for all the structures was measured as  $2 \times 10^{12} \text{ cm}^{-2}$ .

Channel thickness (nm)	Mobility ( $\text{cm}^2/\text{V s}$ )					
	As-grown		Annealed at 650 °C		Mobility enhancement	
	300 K	10 K	300 K	10 K	300 K	10 K
8	920	7300	1010	11 600	10%	59%
16	1010	7130	1840	26 900	82%	377%
20	1440	8680	1910	19 900	33%	229%
30	1430	8080	1560	7 480	9%	-7%

(650 °C for 30 min). Annealing certainly makes an enormous improvement with the mobility of the 16 nm channel structure being increased by a factor of almost 4 at low temperature and nearly doubled at RT.

The plan view TEM images show that annealing also allows the misfit dislocations to move away from the regular cross hatch pattern, seen immediately after growth in Fig. 5(b), to the more irregular serpentine pattern of Fig. 7. This tends to produce larger areas that are free of dislocations but other regions where the dislocations cluster, so the overall effect on mobility remains to be investigated. Meanwhile the small surface ripples between the cross-hatch patterns appear to be unchanged. The dislocation density and plastic relaxation were obtained after annealing at 650 °C and are compared with those from the as-grown structures in Table II. Although annealing led to some relaxation, seen through an increase in  $\rho_{\text{ML}}$ , this was less than 5% for the three narrowest channels and it produced a significant improvement in mobility, particularly at low temperature. However, in the case of the 30 nm layer the relaxation was estimated to exceed 20% both before and after annealing, which made no real improvement in mobility. At this point some of the strain induced benefits such layers are designed to incorporate would be lost. The fact that it was relaxed, and so had far more misfit dislocations present, is apparently more important for suppressing the electrical properties than any effect of point defects.

Figure 8 depicts the variation of Hall mobility with channel thickness after annealing. This shows there is an optimal thickness in the range 15–20 nm below which the

rough upper interface limits the hole mobility and above which relaxation and dislocations dominate. At room temperature there is a smaller variation with channel thickness than at 10 K suggesting that the effect of misfit dislocations is less influential and is masked by a greater contribution from optical phonon scattering, which has been shown to be a major RT scattering mechanism in similar structures.<sup>19</sup>

To investigate the effects of annealing on interface quality and atomic diffusion, SIMS analysis was performed, using low energy (500 eV)  $\text{O}_2^+$  ions to optimize the depth resolution.<sup>20</sup> Figure 9 shows low energy SIMS profiles for the 16 nm channel sample (which are indicative of those observed for all the structures) before and after annealing. From these profiles, the amount of Si diffused into the Ge channel and the degree to which the channel spreads can be obtained (Fig. 10). For the structures annealed at 600 °C the channel width and shape is essentially unaltered from the as-grown material, but there is a small amount of Si diffusion at the lower interface. This is evidence that atoms have moved within the lattice to eliminate the point defects and Fig. 3 shows that the electrical qualities have clearly improved. As the anneal temperature is increased more Si diffused across each interface leading to a smearing of the interfaces by up to 1 nm for the 700 °C anneal (Fig. 10). There is much less evidence that the Ge atoms diffuse far into the Si, which is to be expected as the diffusion coefficient for Si in Ge is much higher than that of Ge in Si.<sup>21</sup> The amount of diffusion was also found to depend on the channel thickness for a particular anneal temperature—more Si was observed

TABLE II. Measured misfit dislocation line density and estimated channel relaxation in the as-grown and 650 °C annealed samples, along with the amount of Si diffused into the Ge channel estimated from SIMS analysis.

Channel thickness (nm)	As-grown		Annealed at 650 °C		
	Misfit dislocation density ( $\text{cm}^{-1}$ )	Estimated channel relaxation (%)	Misfit dislocation density ( $\text{cm}^{-1}$ )	Estimated channel relaxation (%)	Estimated Si diffusion into Ge channel (%)
8	...	...	...	...	6
16	$1 \times 10^3$	0.2	$1.5 \times 10^4$	3	3
20	$4 \times 10^3$	0.8	$2.5 \times 10^4$	5	2
30	$>10^5$	$>20$	$>10^5$	$>20$	$<1$

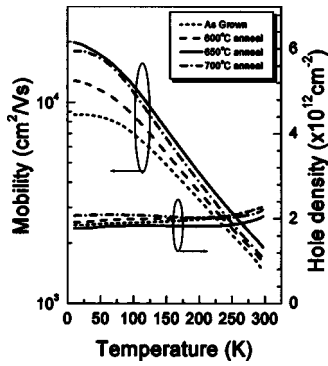


FIG. 6. Hall effect measurements of the hole mobility and density as a function of temperature for the 20 nm channel structure, as-grown and annealed at 600, 650, and 700 °C.

for thinner channels. At 650 °C, the temperature found to yield the best electrical properties, the amount of Si present in the center of the Ge channel varied between 6% for the 8 nm structure and <1% for the 30 nm one (Table II). For higher anneal temperatures (700 °C) the amount of Si diffusion increased significantly with 4% in the 30 nm structure and 14% in the 8 nm structure. The accompanying smearing of the interfaces in this latter sample might be expected to lead to a loss of confinement and two-dimensional hole gas behavior. The scale of diffusion at 700 °C also accounts for a drop in mobility seen with the 16 and 20 nm structures, as the quality of the interface that the carriers are confined against will degrade along with the possible introduction of alloy scattering. Despite this Si diffusion, Fig. 6 shows that the hole density does not change significantly with annealing suggesting minimal out-diffusion of the doping supply layer.

VI. SUMMARY

This work has demonstrated that Ge channel heterostructure growth requires very stringent conditions. Both the growth temperature and thickness of the layers play a significant role in the overall material properties. It has been shown

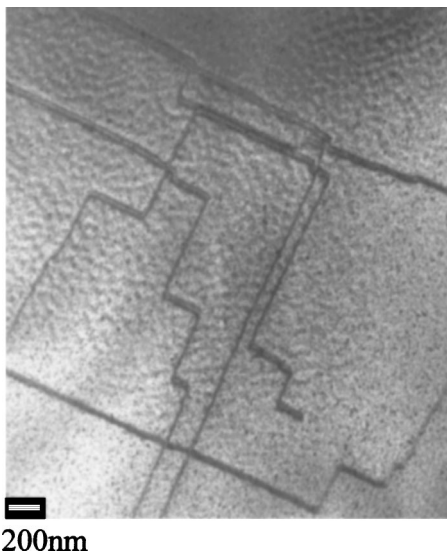


FIG. 7. Plan view TEM image of the 20 nm channel structure after annealing at 650 °C.

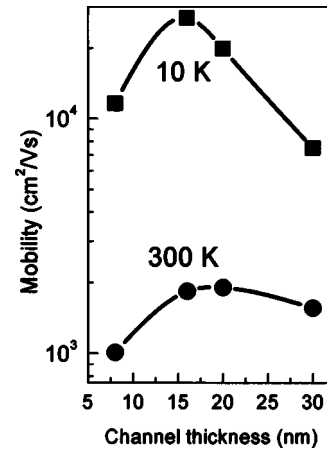


FIG. 8. Variation with Ge channel thickness of the Hall mobility measured at 10 and 300 K for annealed samples.

that for too high a growth temperature ( $\geq 400$  °C) the Ge layer severely roughens. The roughening takes the form of facets which is common for the SiGe material system. For layers of equilibrium critical thickness or less, such roughening of the channel interface will be highly detrimental to the electrical properties, since both interfaces influence hole motion in these narrow channels.

By lowering the growth temperature to below 350 °C this roughening is suppressed, but the as-grown material quality appears to be compromised. However, subsequent annealing at 650 °C under dry N<sub>2</sub> was shown to result in significant improvements to the electrical properties, especially at low temperature where the mobility was enhanced by factors up to 4. This observation strongly suggests that point defect nucleation had occurred and that the damage is removed by annealing. Diffusion of Si from the cladding layers into the Ge channel was found after annealing, but this appeared to have almost no detrimental behavior on the material's electrical properties for anneal temperatures up to 650 °C. Previously, work on similar Ge channel structures found that *in situ* annealing degraded the electrical behavior,<sup>22</sup> but the results presented here show that *ex situ* annealing under the right conditions enhances the hole carrier properties. These results also imply that the structures

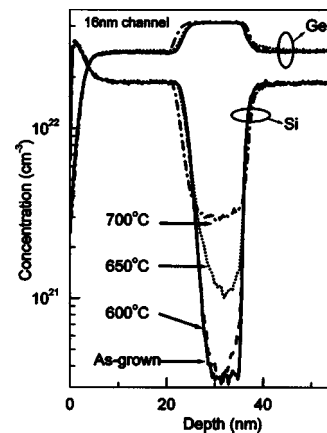


FIG. 9. Si and Ge SIMS profiles of structures with a 16 nm Ge channel showing the diffusion of Si atoms on annealing.



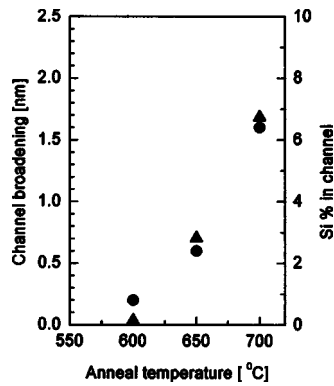


FIG. 10. Showing the increase in effective Ge channel thickness (triangles) and percentage of Si diffused into the center of the channel (circles) as a function of anneal temperature, obtained from the SIMS data in Fig. 6.

are resilient to thermal cycling up to 650 °C, which is important when considering processing devices from such material.

1D Poisson/Schrödinger modeling suggested that the influence of a rough upper interface could be reduced by increasing the Ge channel thickness up to and beyond the critical thickness. While this did lead to a substantial improvement in mobility, especially after annealing, it was found to introduce another problem—the formation of misfit dislocations. Hall measurements at 10 K indicated that these misfit dislocations have a strong influence on the hole mobility, which deteriorated with increasing channel width beyond the equilibrium thickness. TEM measurements showed a corresponding increase in the misfit dislocation line density, from which the amount of plastic relaxation was estimated and found to increase rapidly with layer thickness.

In conclusion, we see that strained Ge can offer large hole mobility enhancements, ideal for *p*MOS devices, but to fully realize these benefits of good quality strained Ge layers must be grown. The growth temperature, channel thickness,

and subsequent thermal processing have been shown to be critical in order to obtain the best quality material with the highest hole mobility.

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