

A complex visualization of particle detector data, featuring a dense cluster of small, light-gray rectangular blocks at the center, with numerous thin, curved lines radiating outwards, suggesting particle tracks or detector components.

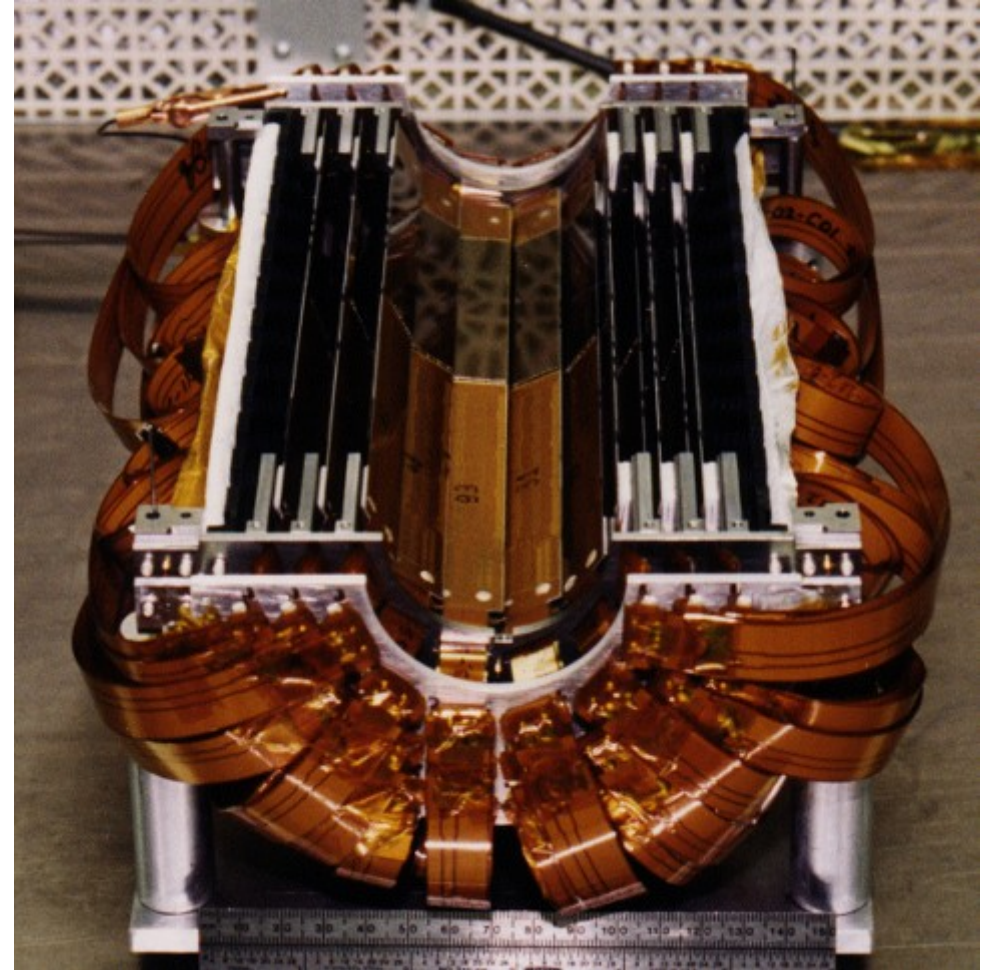
Pixel Technologies for the ~~ILC~~

Generic future Colliders of any shape

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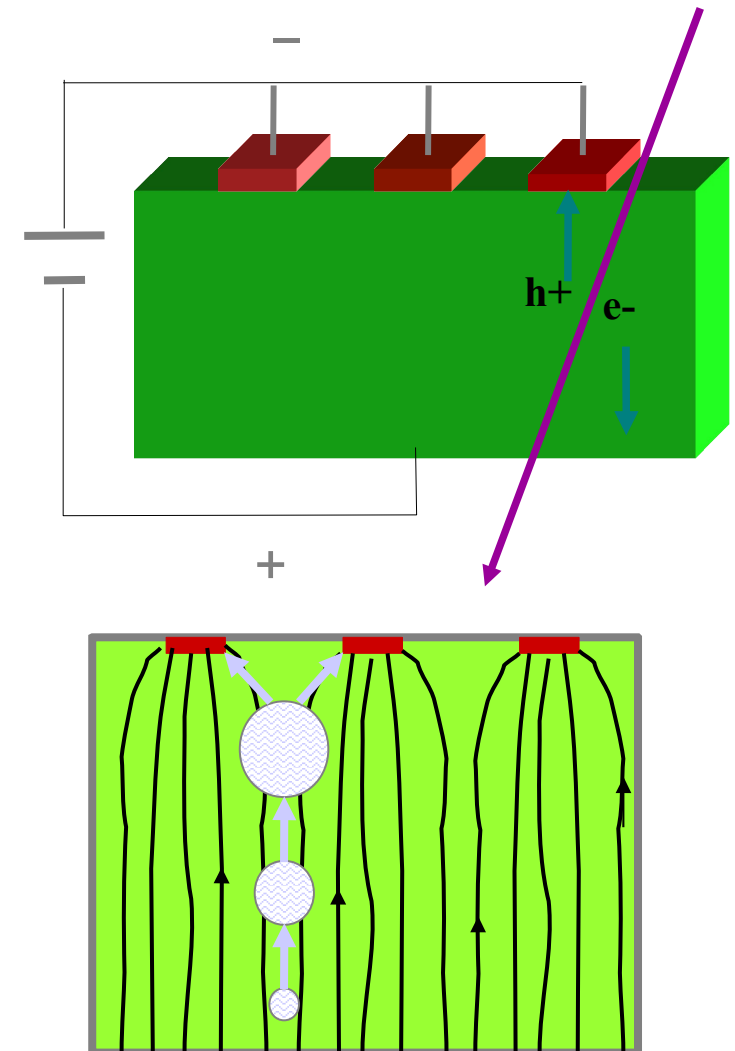
In the beginning ...

- SLD's VXD3 (1996)
 - 307 Million channels
 - 20 μm pixels
- The Grandfather of all LC pixel detectors
- Still provides valuable “lessons learned” from SLC
- Starting point for ILC pixel R&D



How does a Silicon Pixel work ?

- From a semiconductor perspective
 - Silicon pn-junction (aka Diode)
 - not really that different from a strip detector ...
- Particle passing through
 - always treated as MIP
 - generate electron-hole pairs
 - 80 e/per μm
- Reverse bias pn junction
 - can fully deplete bulk
 - either collect holes or electrons



© Rainer Wallny

Materials

- **High resistivity Silicon**

- $R = 1\text{k}\Omega\text{cm}$
- used mostly for detectors
- Quite expensive
- Charge Collection
 - thickness up to 500 μm
 - Fully depleted
 - Collect charge via drift
 - Fast ($\sim 10\text{ ns}$)
 - small charge spread

- **Low resistivity Silicon**

- $R = 10\Omega\text{cm}$
- Used in CMOS industry (epi)
- Cheap
- Charge collection
 - thin (10 μm)
 - basically undepleted
 - collect charge via diffusion
 - Slow ($\sim 100\text{ ns}$)
 - larger charge spread

Reality is more complex !

There are more things between p and n,
Horatio, than are dreamt of in
your philosophy !

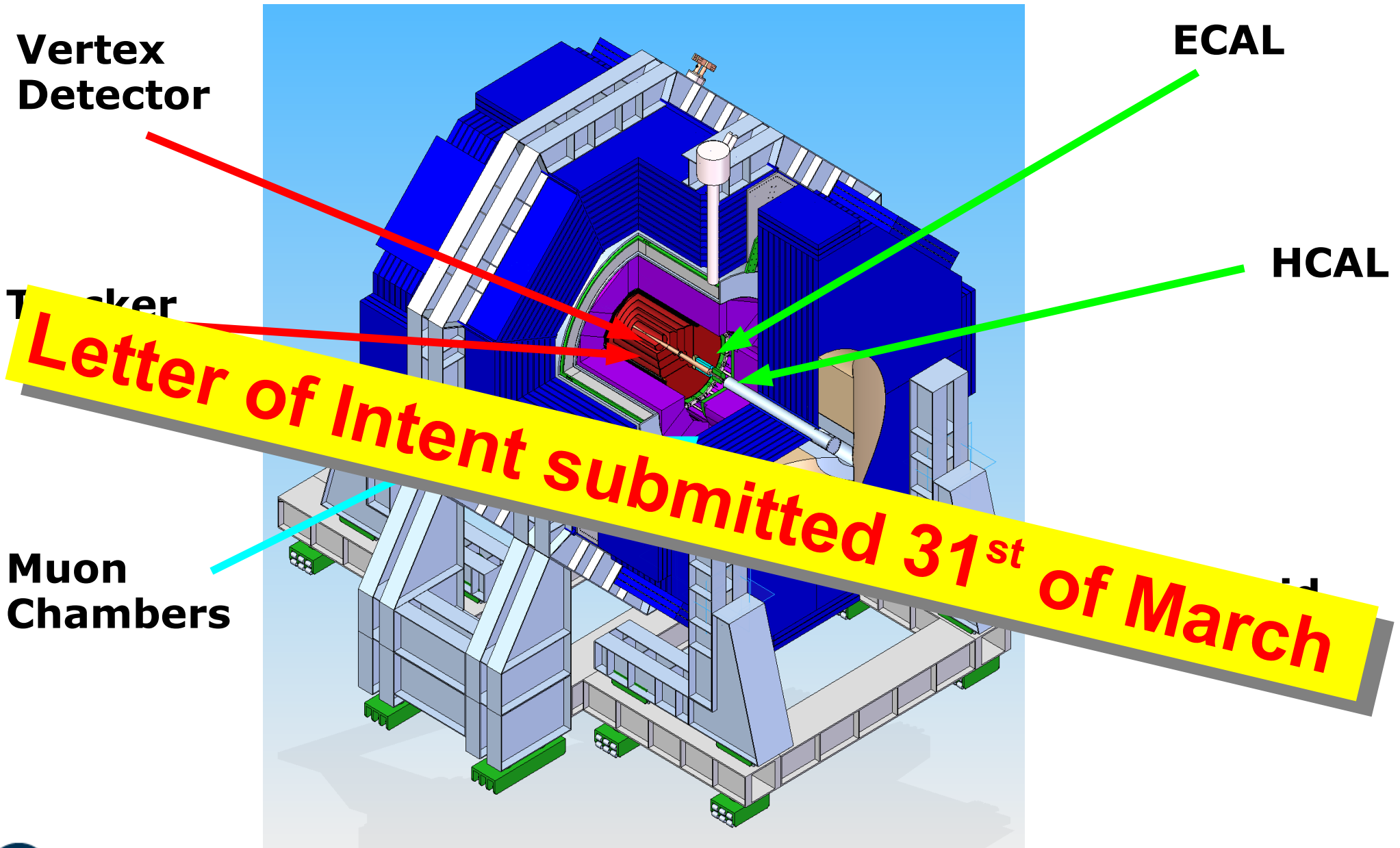


Pixel RD for the ILC

- Very active field for the last ten years
- Plenty of groups involved in all 3 ILC regions
 - Europe
 - Asia
 - Americas
- A lot of progress has been made
- I'll focus on
 - Pixel technologies
 - Silicon-only pixels
- Apologies in advance for omissions ...



SiD - a typical ILC detector



ILC Detector Requirements

- Impact parameter resolution • Need factor 3 better than SLD

$$\sigma_{r\phi} \approx \sigma_{rz} \approx 5 \oplus 10 / (p \sin^{3/2} \theta)$$

$$\sigma_{r\phi} = 7.7 \oplus 33 / (p \sin^{3/2} \theta)$$

- Momentum resolution • Need factor 10 (3) better than LEP (CMS)

$$\sigma\left(\frac{1}{p_T}\right) = 5 \times 10^{-5} \text{ (GeV}^{-1}\text{)}$$

- Jet energy resolution goal • Need factor 2 better than ZEUS

$$\frac{\sigma_E}{E} = \frac{30\%}{\sqrt{E}}$$

$$\frac{\sigma_E}{E} = \frac{60\%}{\sqrt{E}}$$

- Detector implications

- Calorimeter granularity
- Pixel size
- Material budget, central
- Material budget, forward

- Detector implications

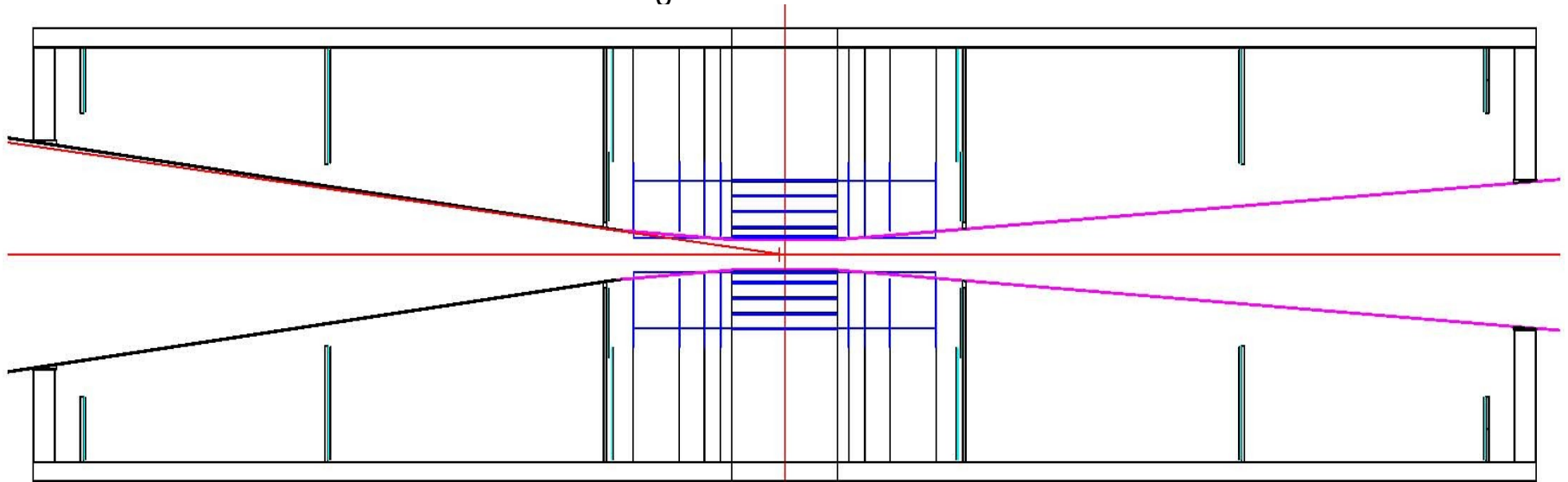
- Need factor ~ 200 better than LHC
- Need factor ~ 20 smaller than LHC
- Need factor ~ 10 less than LHC
- Need factor $\sim >100$ less than LHC

Highly segmented, low mass detectors required -> pixels !



The ILC Vertex Detector

- 5 layers, either
 - long barrels
 - barrels + endcap disks
 - gas-cooled
- First layer ~ 1.2 cm away from primary vertex
- Occupancy 1 %
- Material budget: $\sim 1 \% X_0$

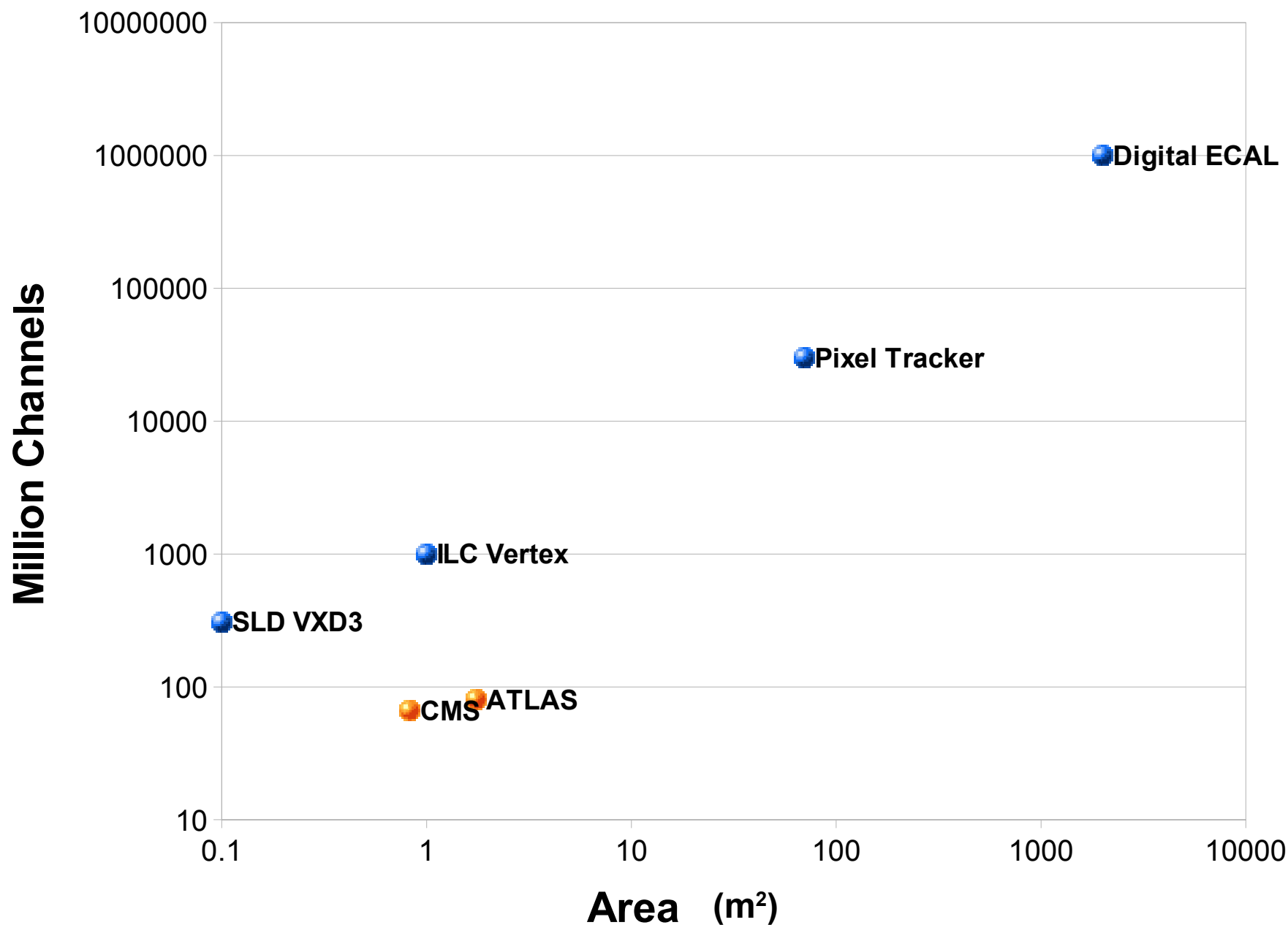


And the pixels spread ...

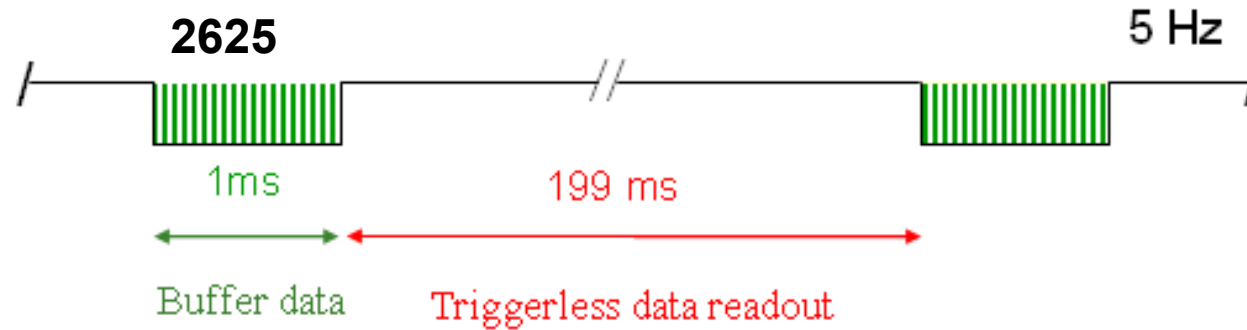
- Pixels originally only intended for the vertex detectors
 - like SLD ...
- But pixels are becoming affordable
 - Pixel detectors spread outwards
- Silicon pixel trackers are now feasible
 - $\sim 70 \text{ m}^2$ silicon , 30 Gigapixel
- Digital EM calorimetry using pixels as particle counters
 - 2000 m^2 area, 1 Terapixel



Pixels everywhere ...



ILC timing



- ILC environment is very different compared to LHC
 - Bunch spacing of ~ 300 ns (baseline)
 - 2625 bunches in 1ms
 - 199 ms quiet time
- Occupancy dominated by beam background & noise
- Readout during quiet time possible

ILC Pixels : Timing and Readout

- Time stamping
 - single bunch resolution
 - buffer hits
 - readout during quiet time
- Time slicing
 - divide train in n slices
 - readout during train/quiet time
- Time-integrating
 - no bunch information
 - readout during quiet time
- On-Pixel processing
 - each pixel self-sufficient
 - digital data stream off pixel
 - minimal amount of interconnects
- Off-Pixel processing
 - data is moved to a readout chip
 - requires additional circuitry and interconnects



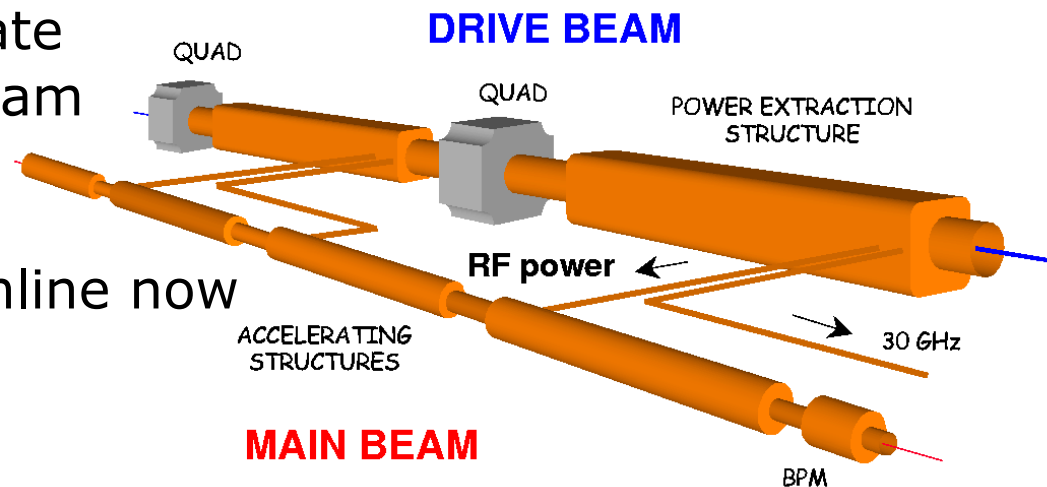
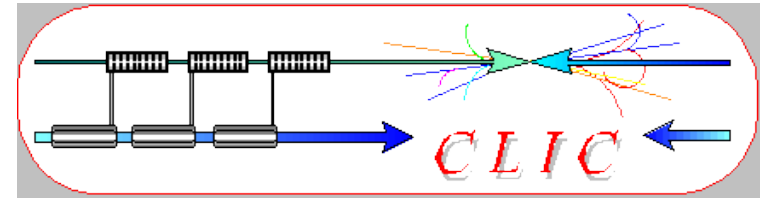
How to achieve Occupancy goal ?

- Goal is 1 % occupancy
 - can't be just done by integrating over the entire train
 - Especially for the inner layers
- Pixel size
 - go to very small pixels
- Time stamping and buffering
 - read and store hits on pixel
- Time Slicing
 - read out the entire detector n times during the train
- Combination of the above



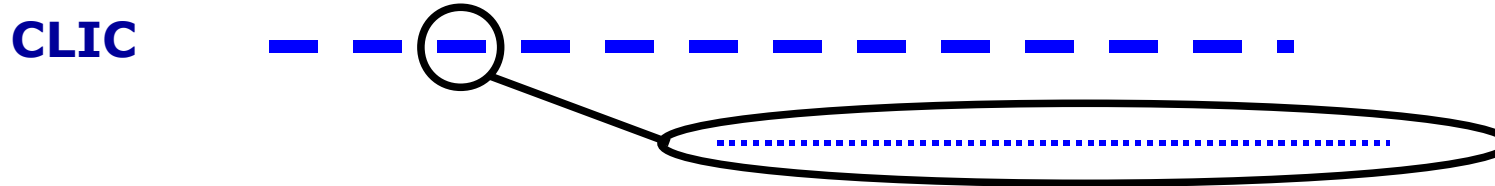
And CLIC ?

- CLIC is an alternative proposal for a linear collider driven by CERN
 - Up to 3 TeV center-of-mass energy
 - 48 km long
- Innovative “Drive-Beam” Technology
 - Drive beam is used to generate accelerating field for main beam
 - Proof -of-principle ongoing
 - CTF3 at CERN is becoming online now
- Very small beams
 - Larger beam backgrounds
 - vertex detector moves outwards (~ 4 cm)



CLIC Bunch structure

Train repetition rate 50 Hz



CLIC: 1 train = 312 bunches

0.5 ns apart 50 Hz

ILC: 1 train = 2680 bunches

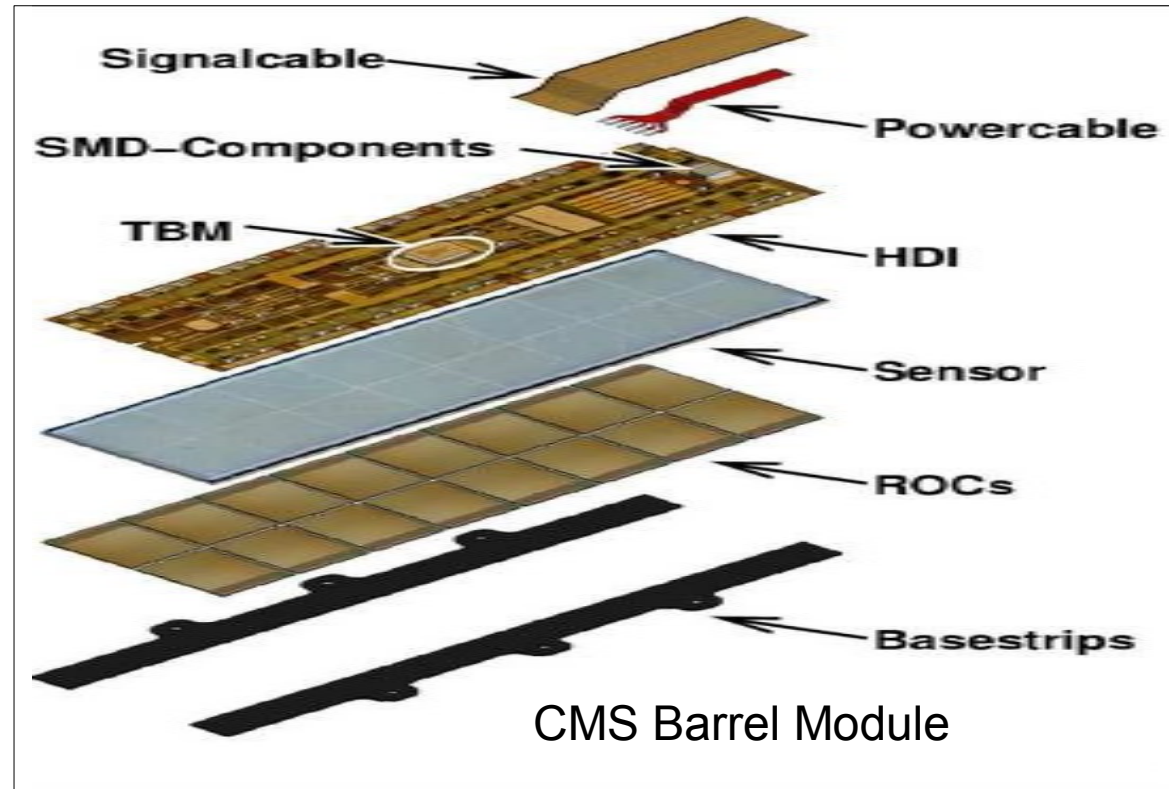
337 ns apart 5 Hz

Consequences for a CLIC detector:

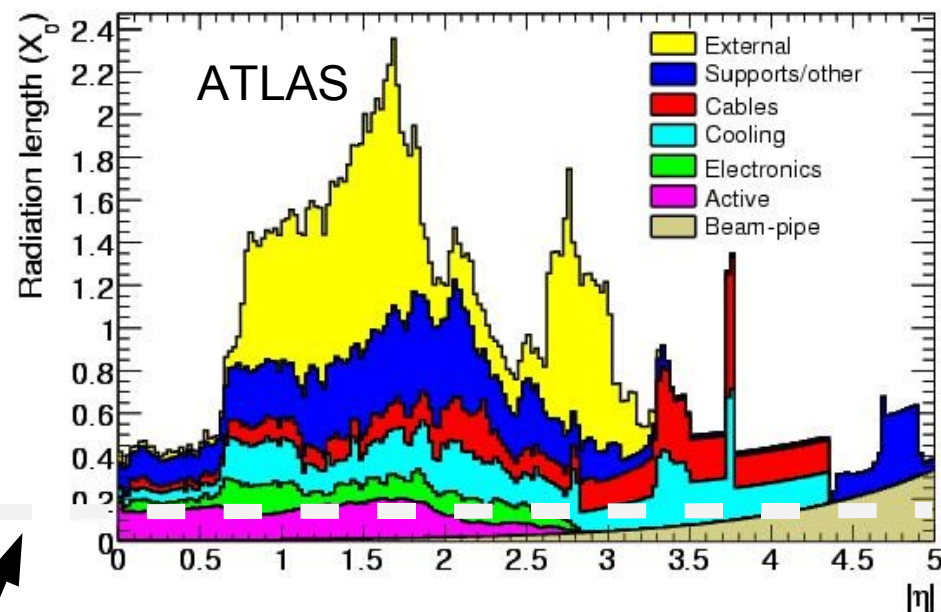
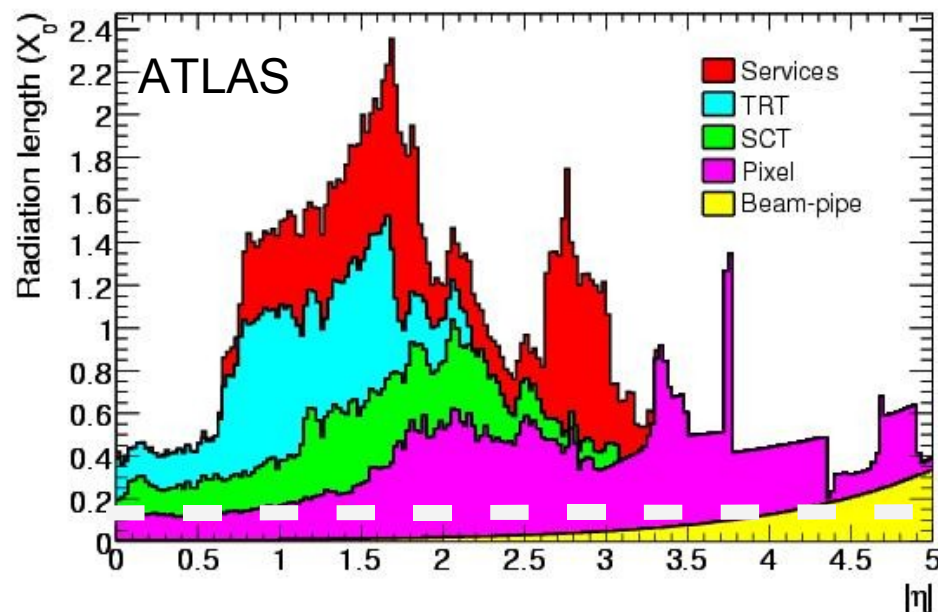
- Assess need for detection layers with time-stamping
 - Innermost tracker layer with sub-ns resolution
 - Additional time-stamping layers for photons and for neutrons
- Readout electronics will be different from ILC
- Consequences for power pulsing?

Why not using LHC-style pixels ?

- LHC requirements
 - extremely rad hard
 - very fast (25 ns)
- LHC pixels ..
 - “large”
 - cooling required
- ILC requirements
 - slow and not rad-hard
- ILC pixels
 - very low material budget
 - high granularity



The material budget



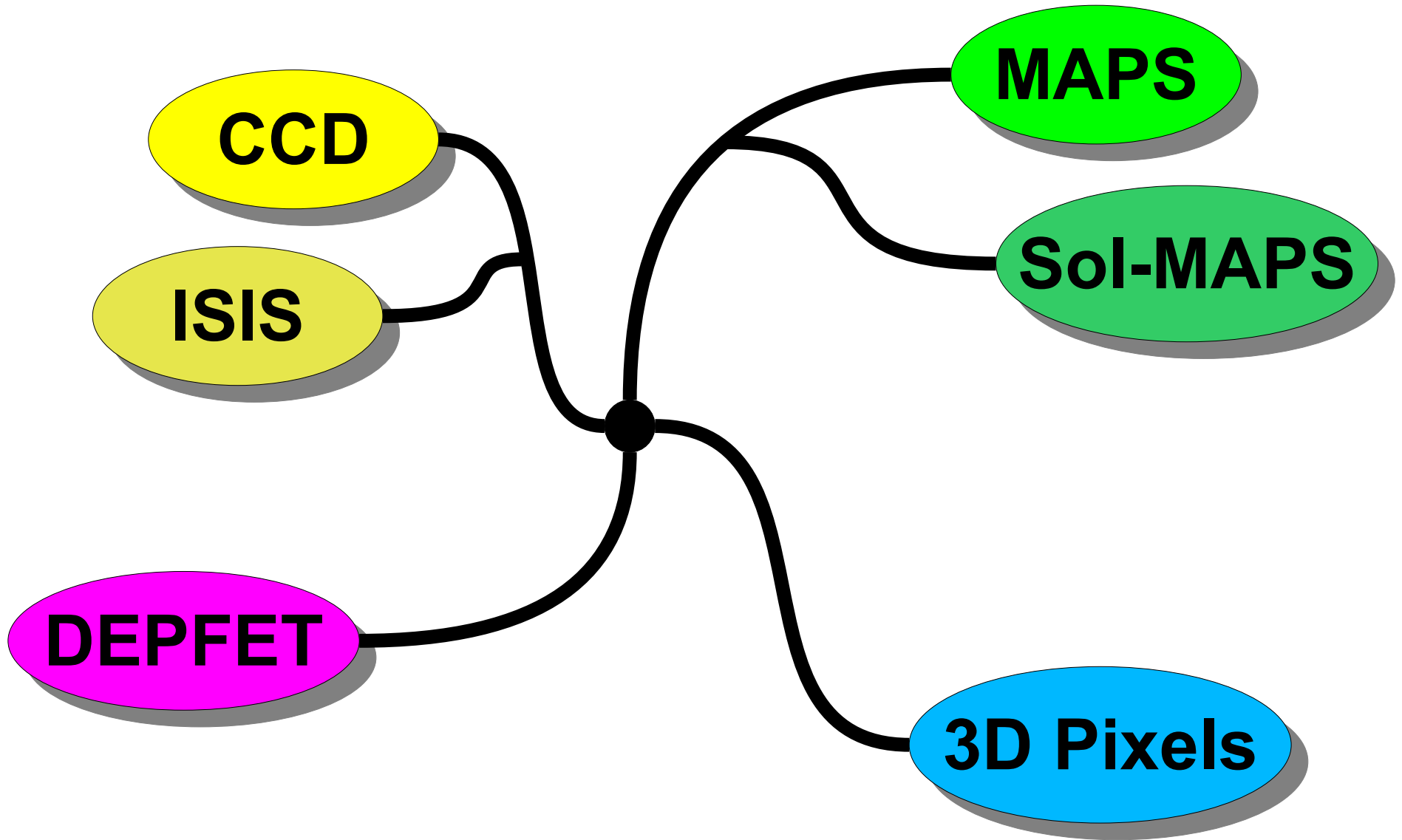
ILC Goal for whole Tracking System

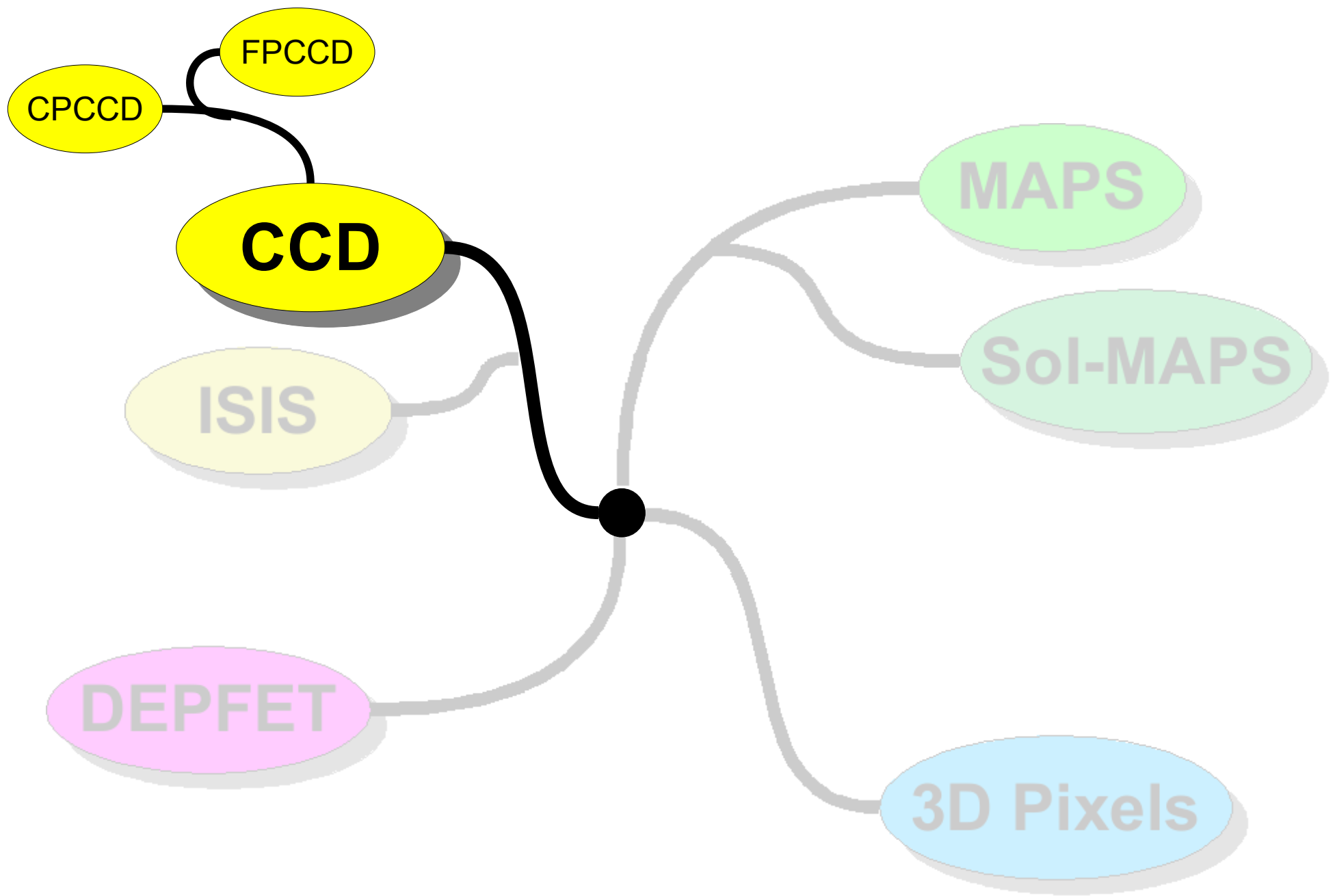
Other short comings

- Excessive use of bump-bonding
 - difficult
 - yield issues
 - limits minimum pixel size ...
- Cooling requirements
 - more material
 - more complexity
- Manufacturing & Cost
 - Everything is custom-made (meaning expensive)
 - Cost per m² too high for large systems



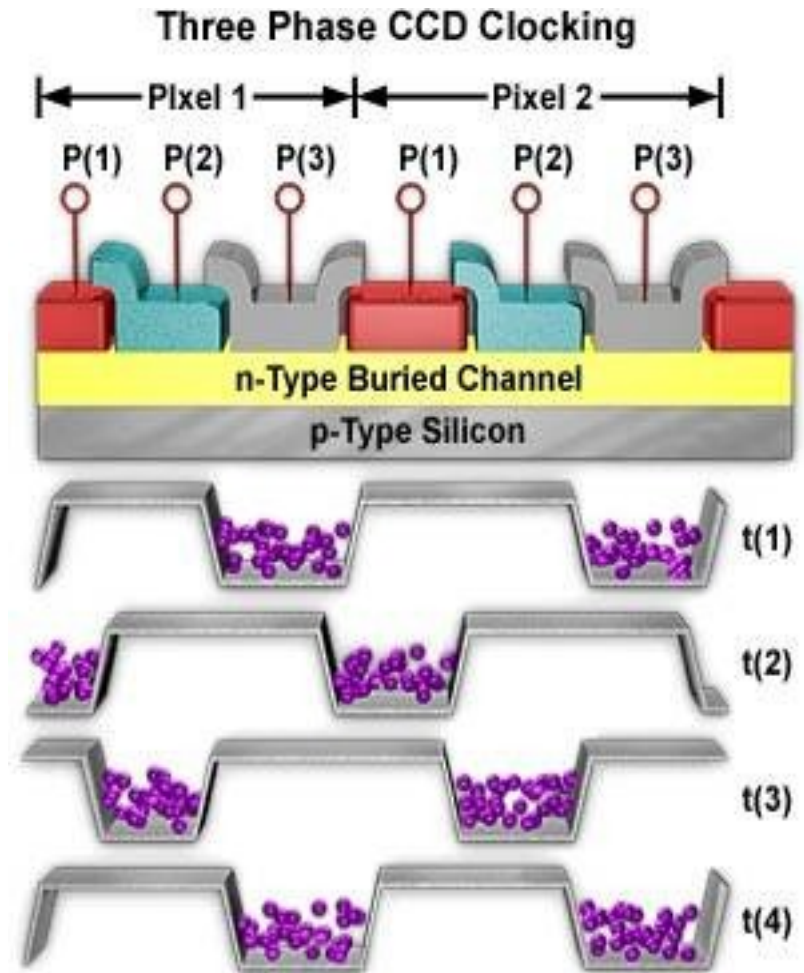
Pixel Technology Tree





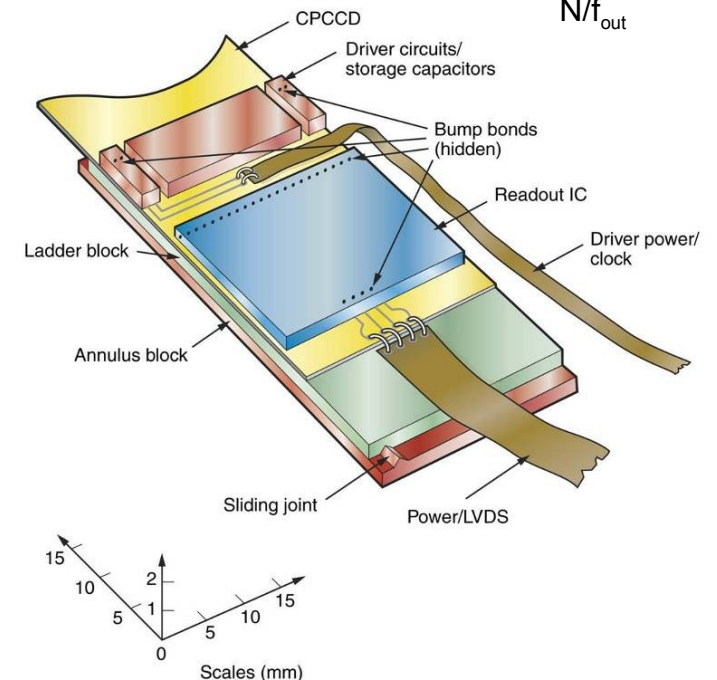
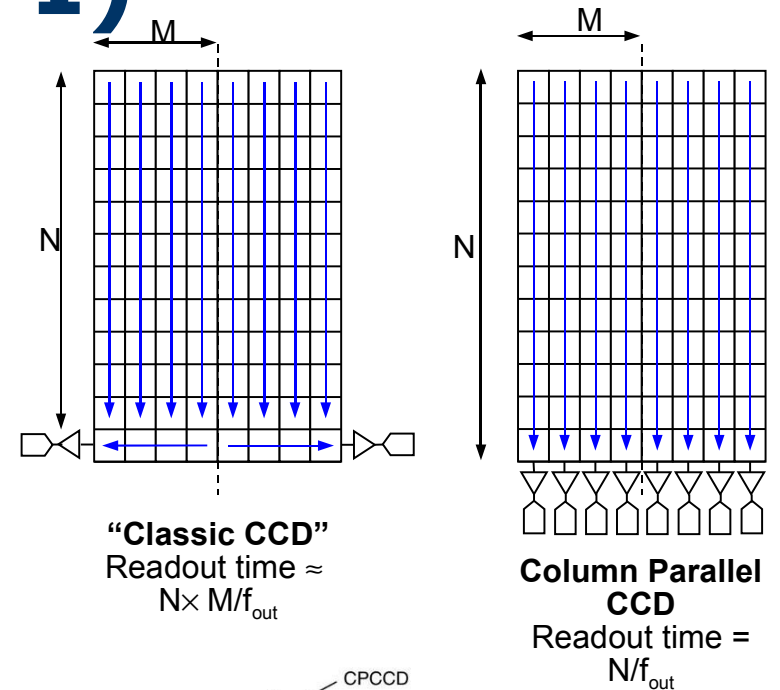
CCD's

- **C**harge-**C**oupled **D**evice
- Extensively used in imaging
- Established technology
- SLD's VXD3 used CCD's
- Basic working principle
 - charge storage
 - readout as bucket-chain
 - robust against pick-up
- Require
 - high charge transfer efficiency
 - cooling to -20 C
 - high drive currents

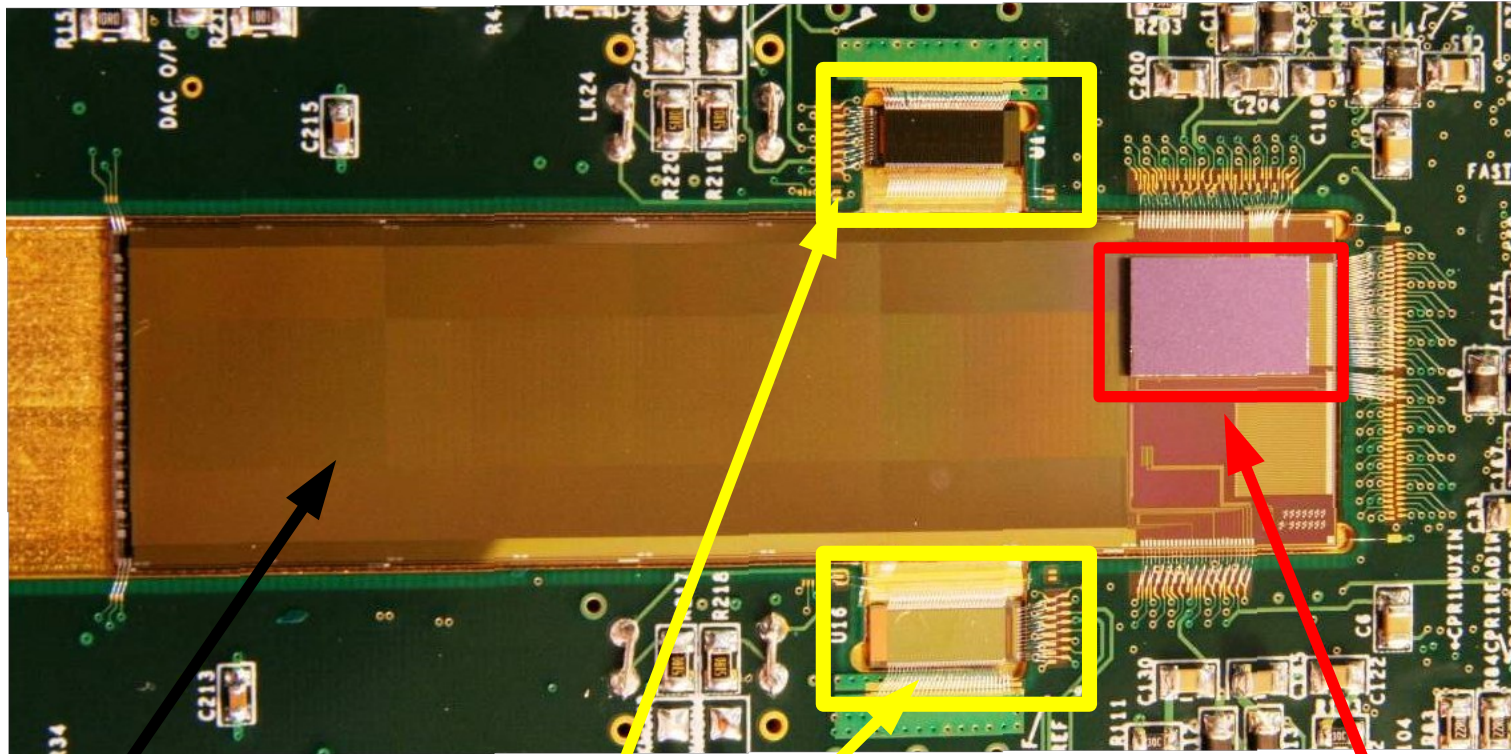


CPCCD (LCFI)

- “Classic ” CCD readout is slow
- **Column Parallel CCD**
- Idea: divide readout chain into columns
 - Higher speeds possible (50 MHz)
 - Time slicing approach (20 frames)
 - 20 μm pixels
- CPCCD requires a dedicated readout chip
- High currents driving the readout
- already second generation design



A CPCCD Module



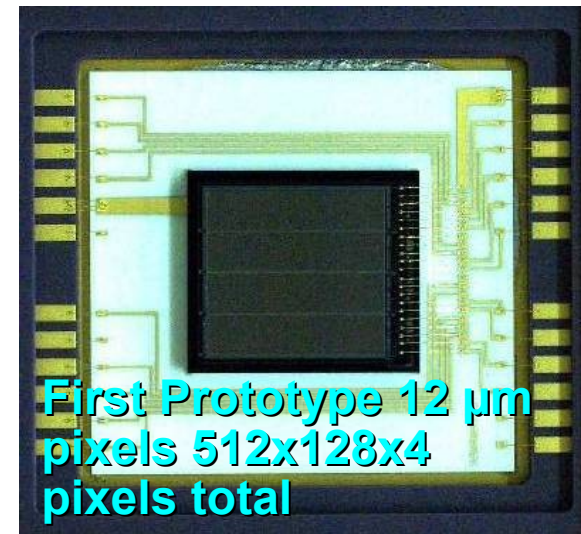
CCD

Driver Chips

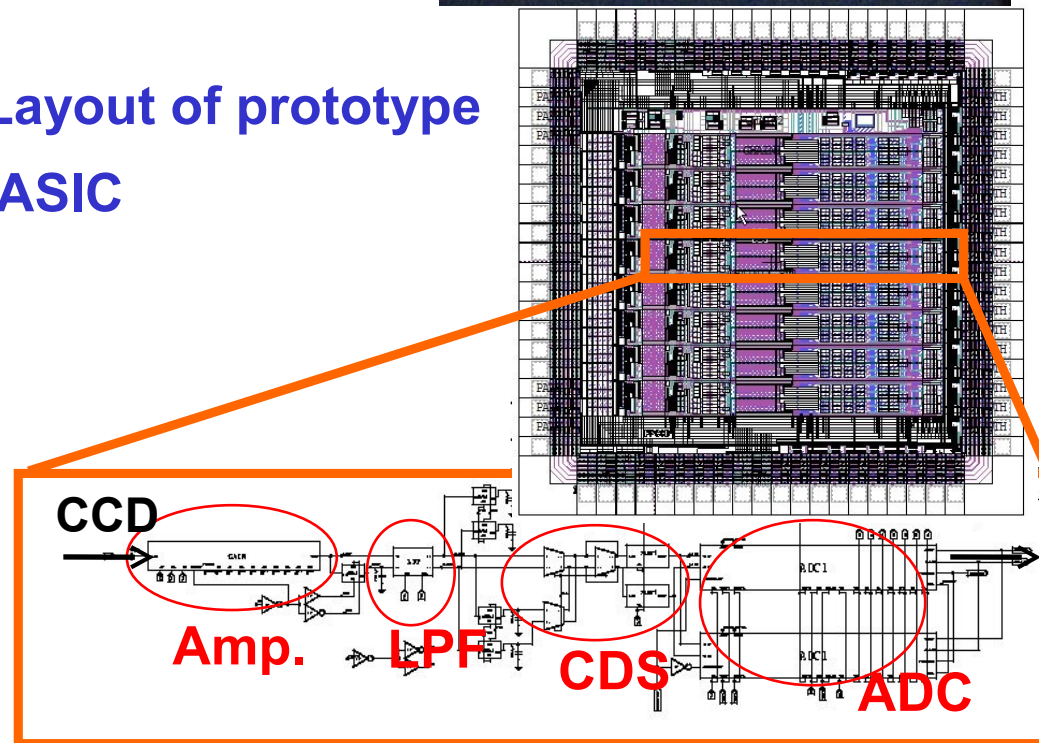
**Readout
ASIC**

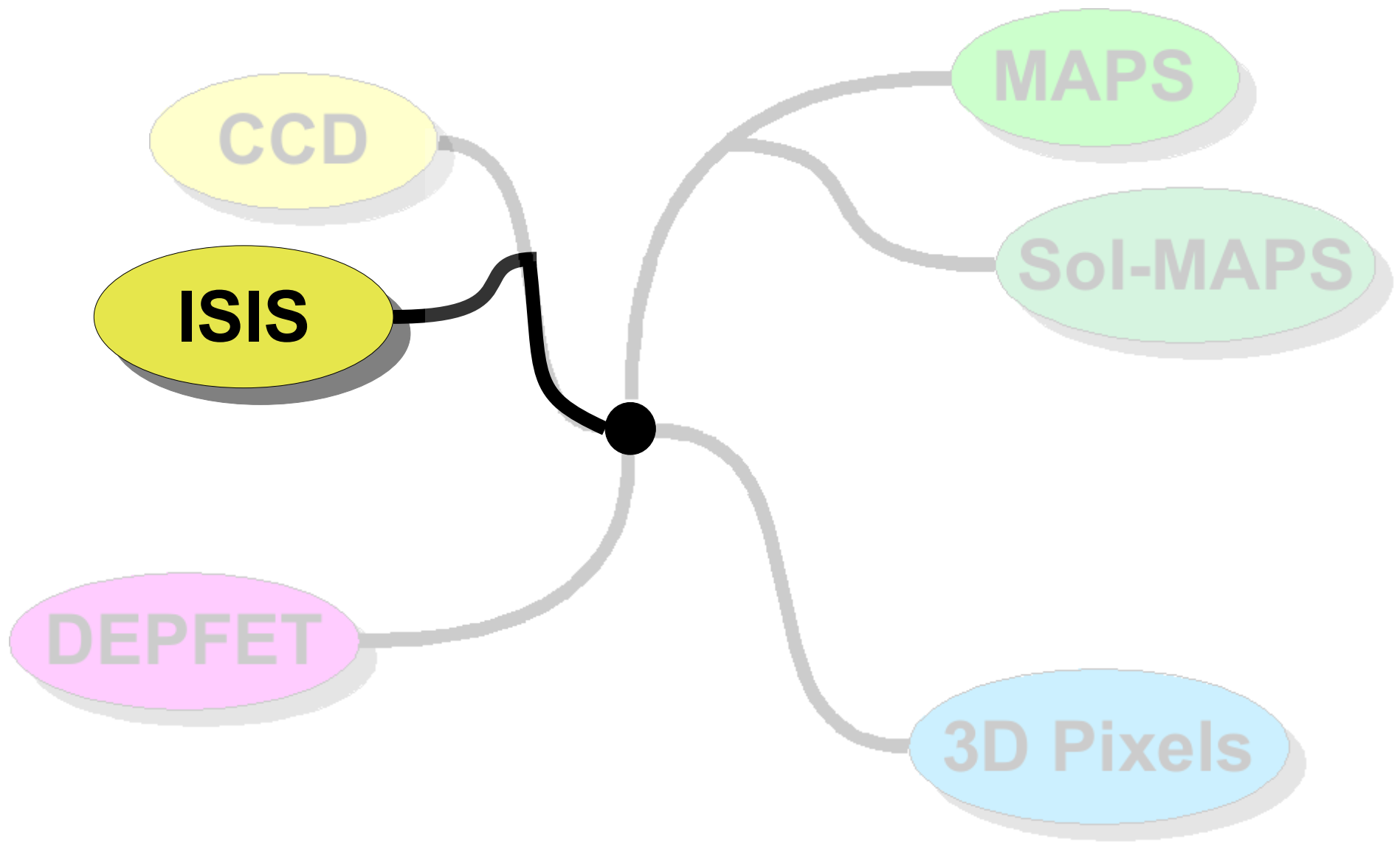
FPCCD (KEK et. al.)

- **F**ine **P**ixel **C**CD
- Time-integrating
 - Instead of time slicing ...
 - requires 5 μm pixels
- Fully depleted epitaxial layer
 - minimize the number of hits due to charge spread
- Requires cooling
- Readout similar to CPCCD
- currently 12 μm pixel size
 - Expect 5 μm pixels in 2011



Layout of prototype ASIC





ISIS (LCFI)

- **In Situ Image Storage**

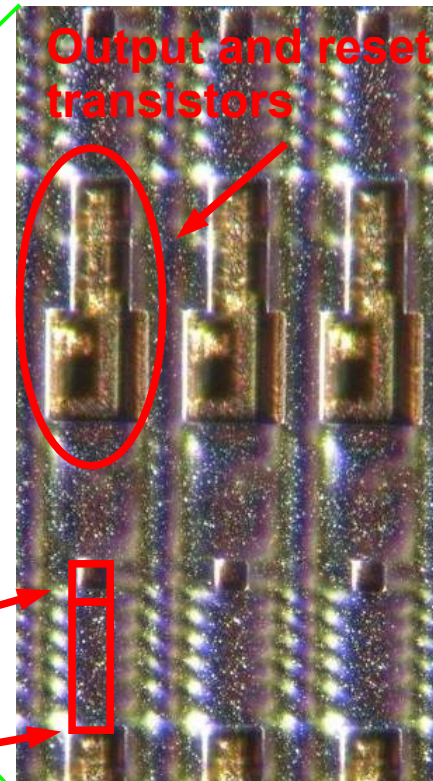
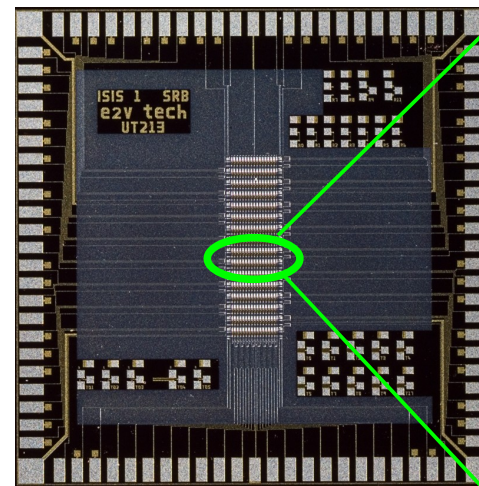
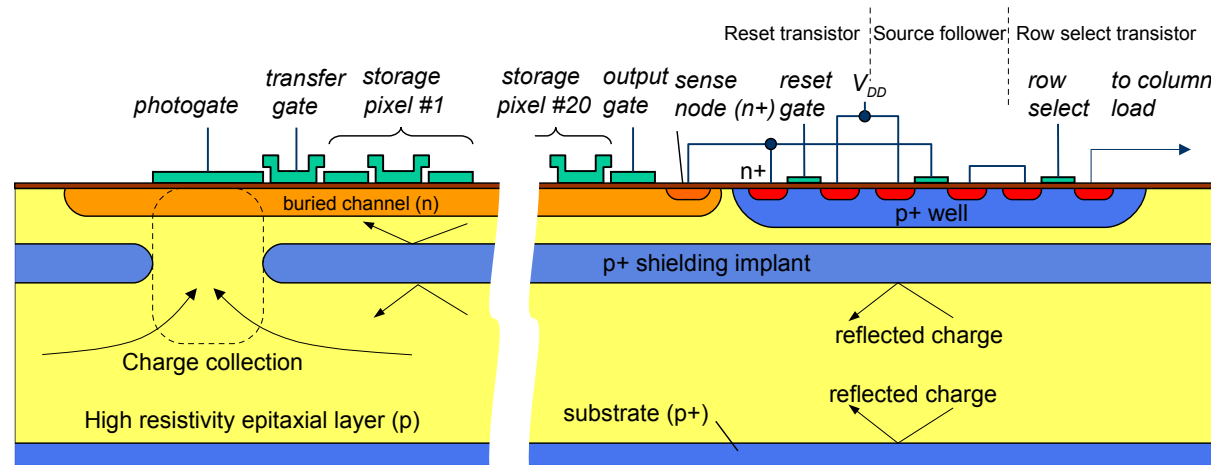
- charge collection with photo diode
- Transfer to CCD-like structure
- Time-slicing (20x)

- Readout chips separate

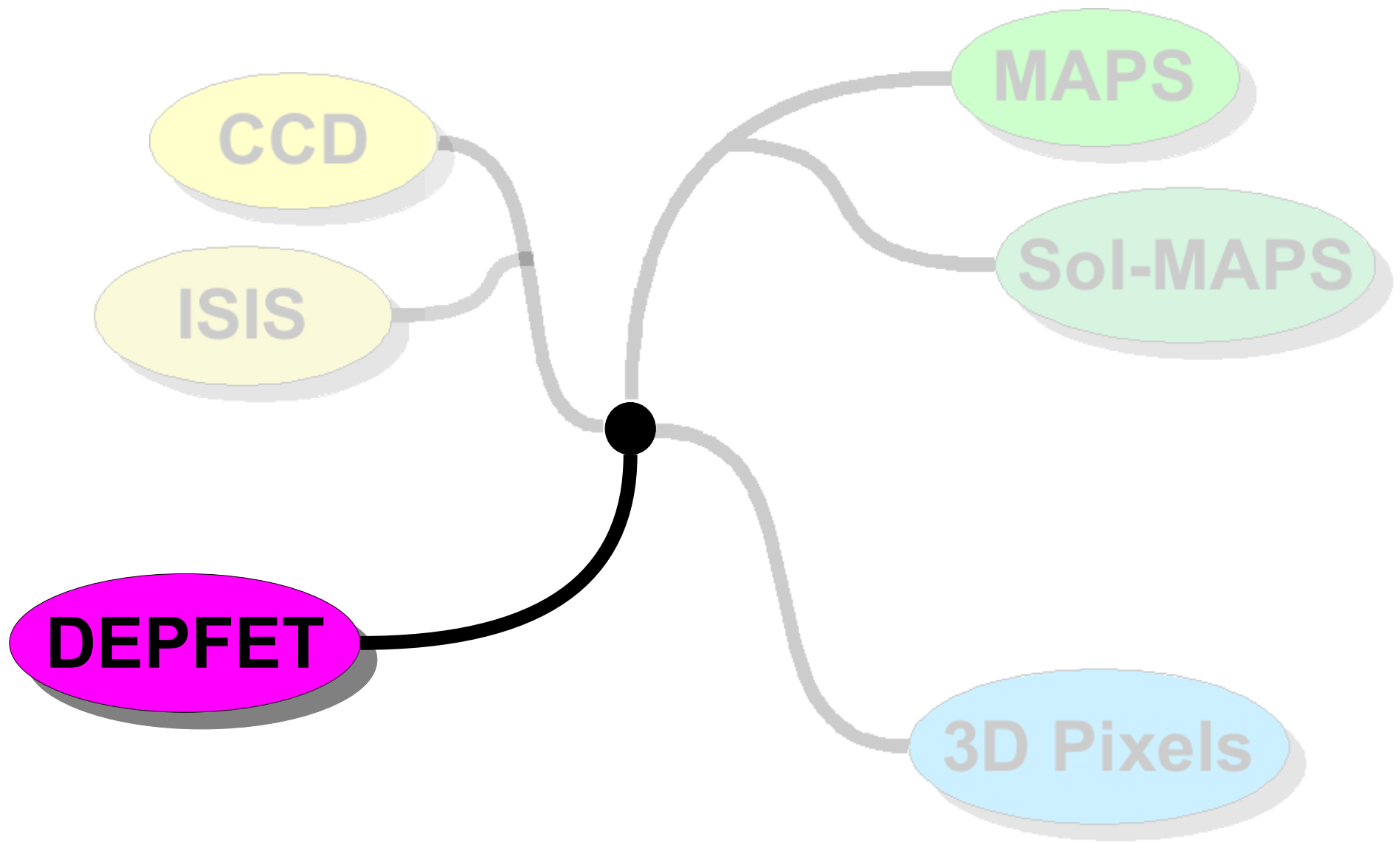
- semi-integrated pixels
- plans for full integration

- First proof of principle devices

- ISIS1
- Successor ISIS2 has shown "signs of life"

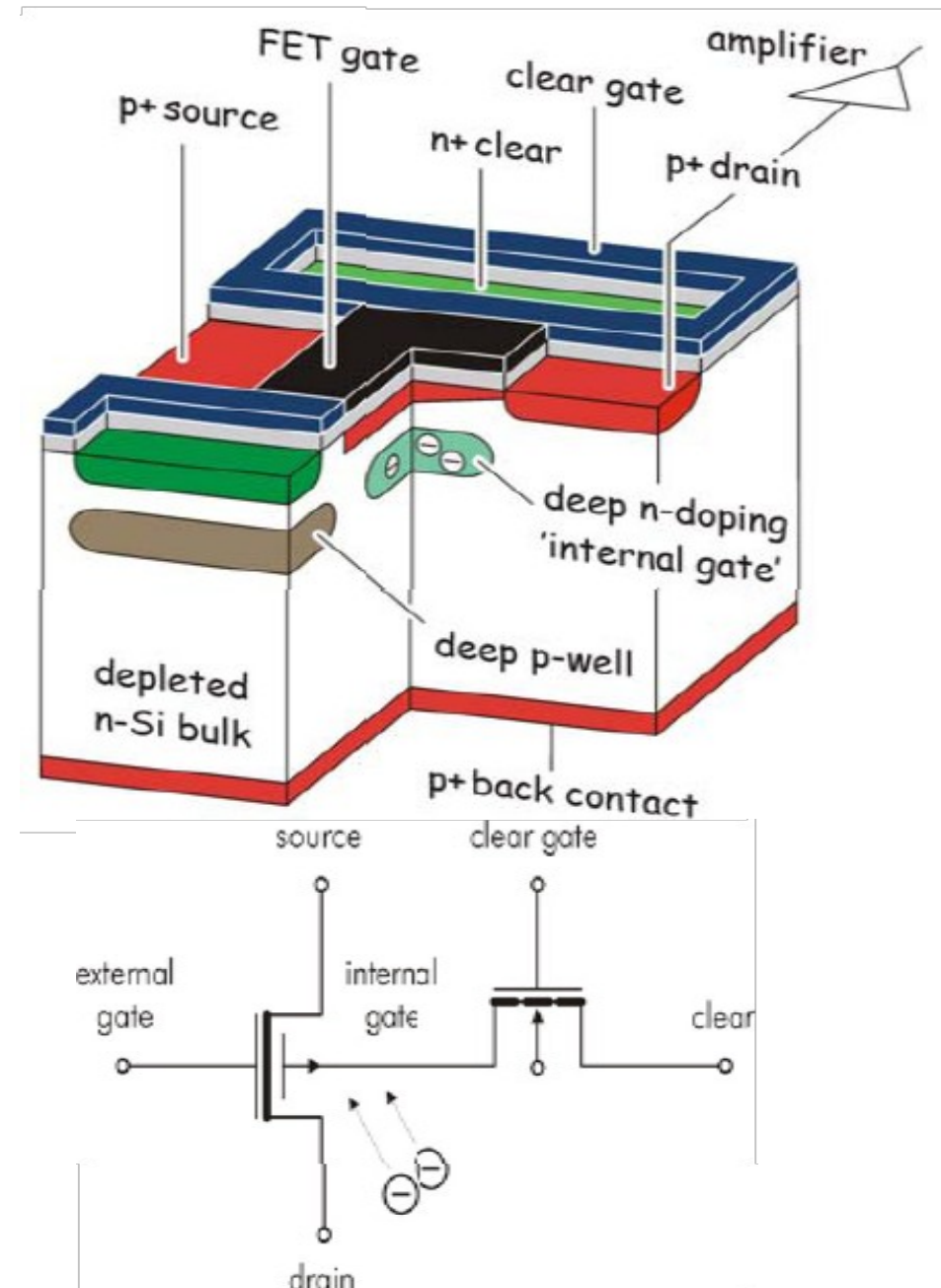


Photogate aperture (8 μm square)
CCD (5x6.75 μm pixels)



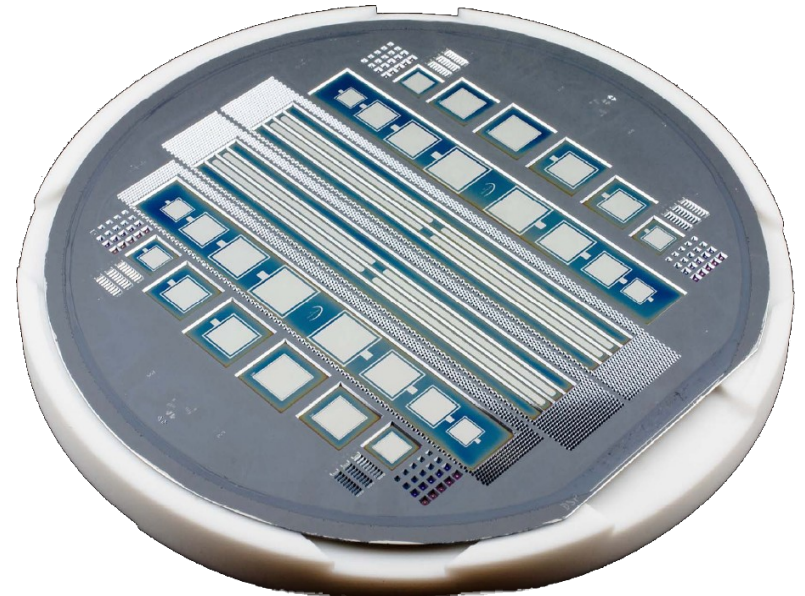
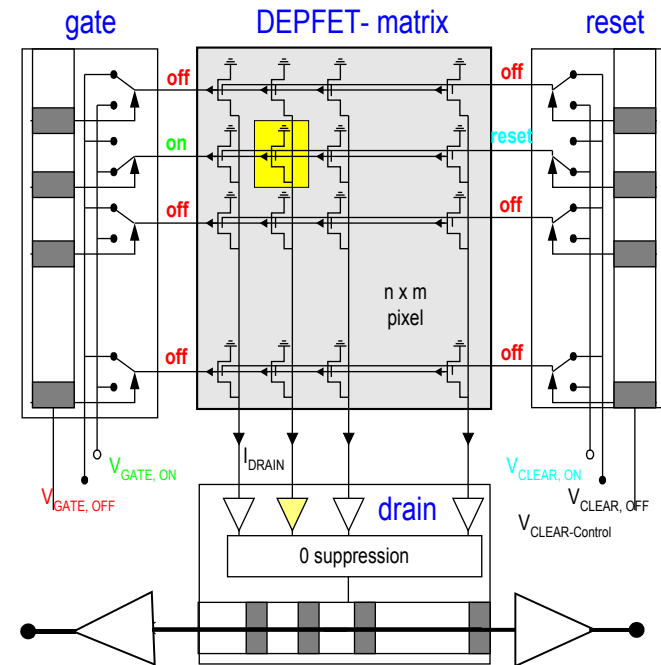
DEPFET (DEPFET collaboration)

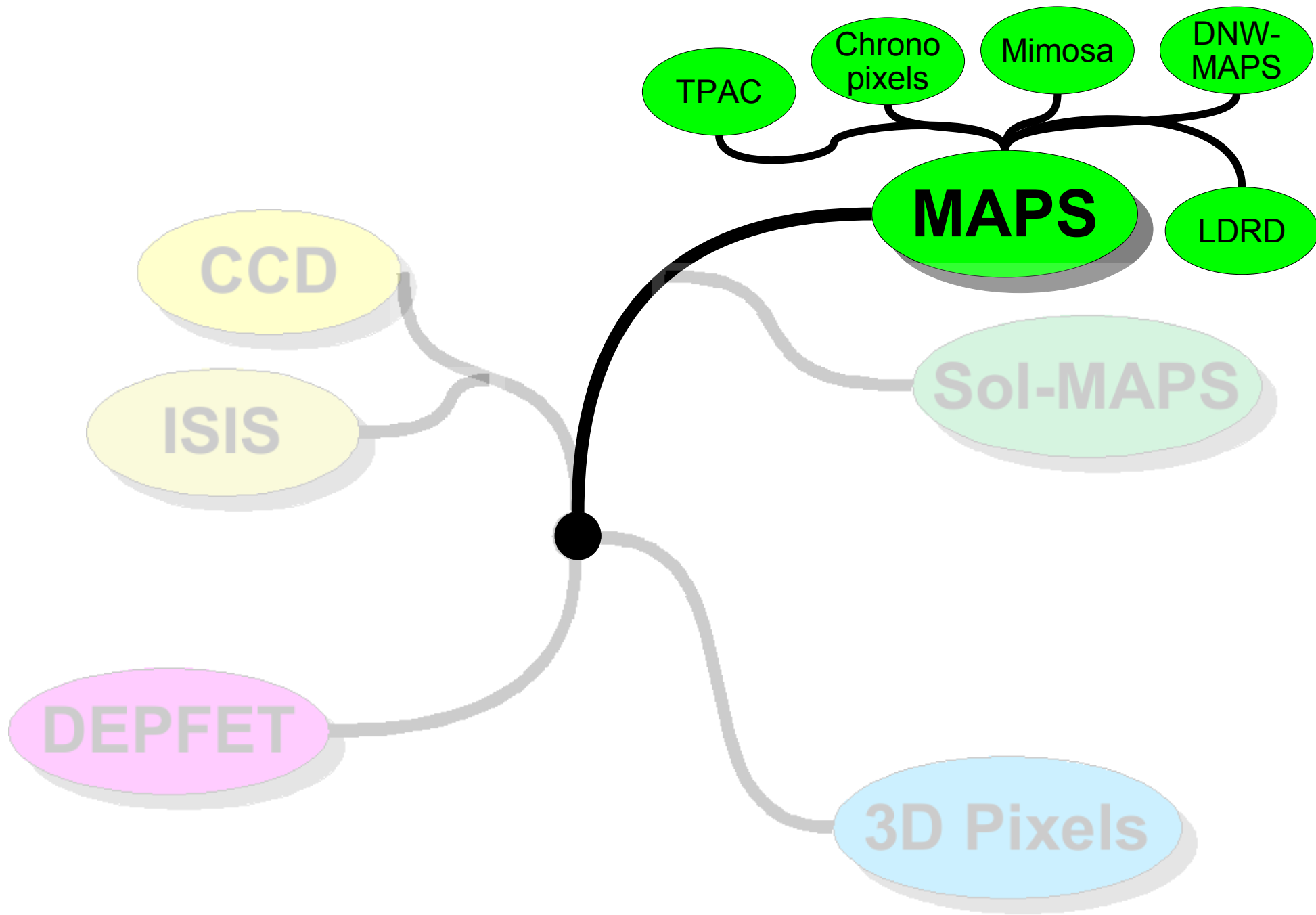
- **DE**pleted **P**-channel **FET**s
- Basic principle
 - Bulk fully depleted
 - Collection by drift
 - Internal gate collects charge
- Clear gate necessary
- Charge collection with FET's switched off, low power
- Unique process developed by MPI Halbleiterlabor München
- Leading Candidate for Super-Belle Vertex Detector



DEPFET Prototypes

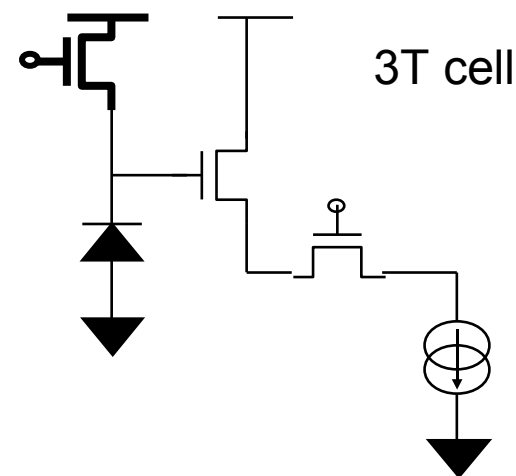
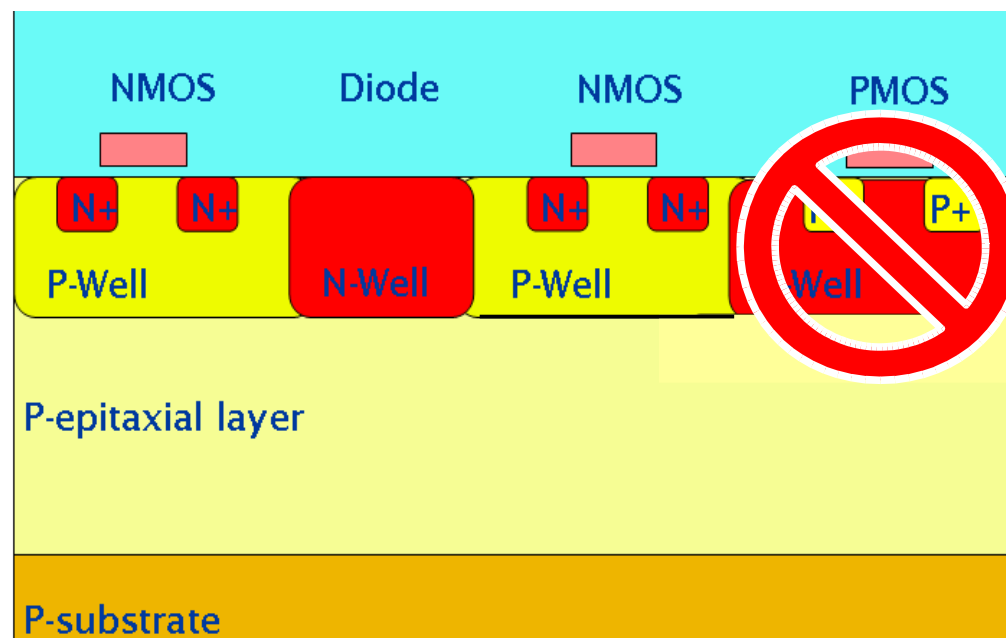
- DEPFET readout
 - External gate row select
 - Signal charge modifies current
 - CDS style readout using Clear gate
- Two driver ASICs needed
- Latest version PXD05
 - 24 μm pixel size
 - tests ongoing





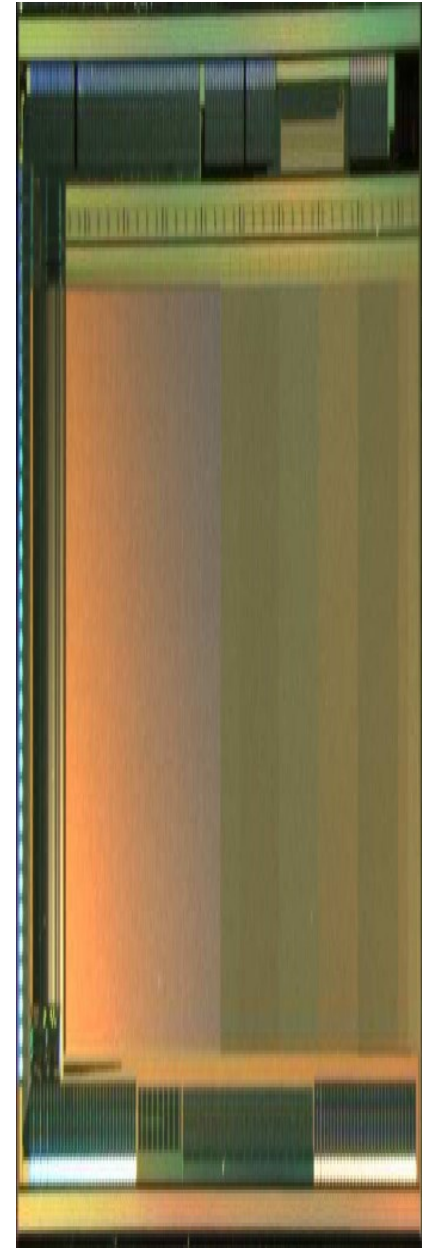
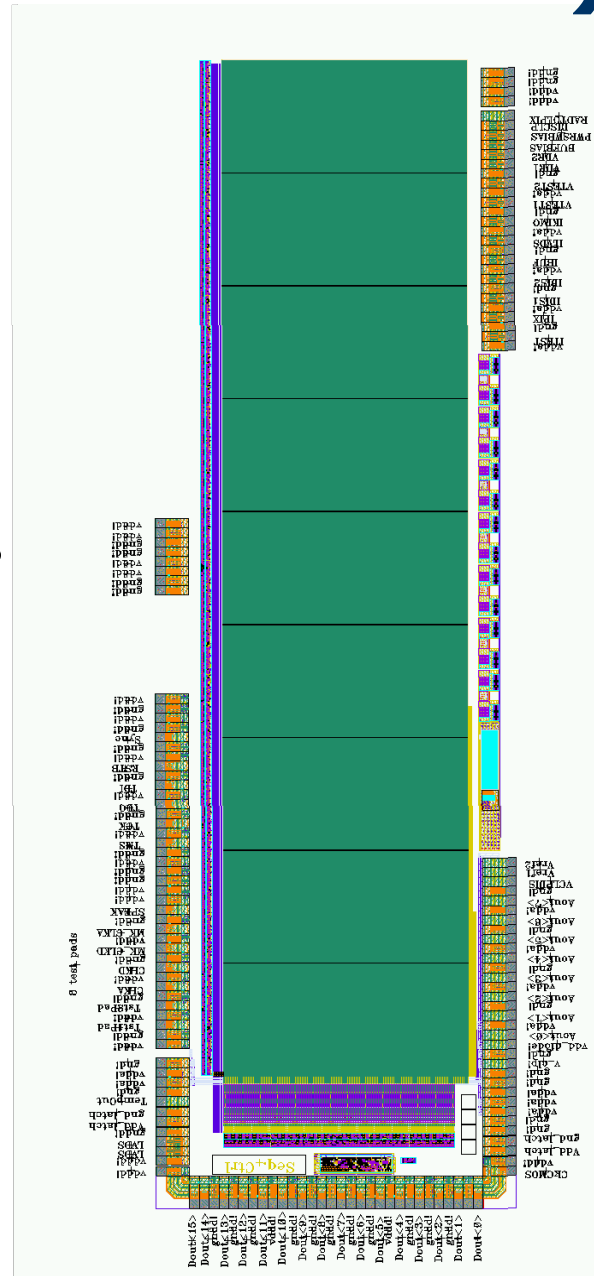
MAPS basic principle

- **M**onolithic **A**ctive **P**ixel **S**ensors
- CMOS technology
 - Down to 180 nm/130 nm
- Charge is collected by diffusion
 - Slow > 100 ns
- Integrated readout
- Thin Epi-layers (< 15 μm)
- Parasitic charge collection
 - can't use PMOS ...
- Basic MAPS cell for Particle Physics
 - The 3T array



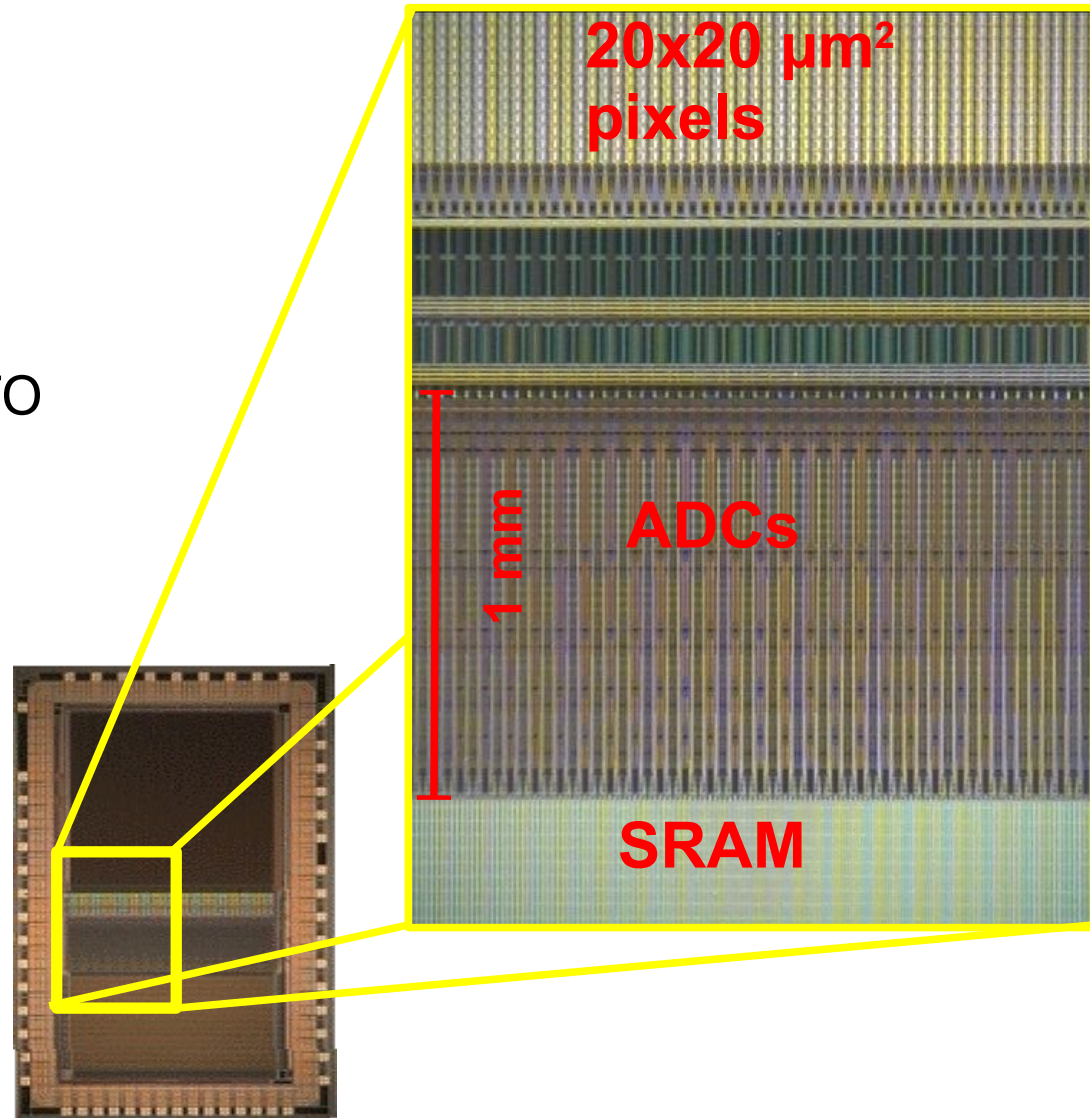
MIMOSA (IRES et. al.)

- MIMOSA family
 - 3T architecture
 - Restricted to NMOS
- MIMOSA 22
 - 0.35 μm AMS OPTO process
 - 18.4 μm pixel size
 - 128 columns
 - 128 x 576 pixels in total
 - Read-out time 100 μs
- Readout as Rolling-Shutter
 - One column read out at a time



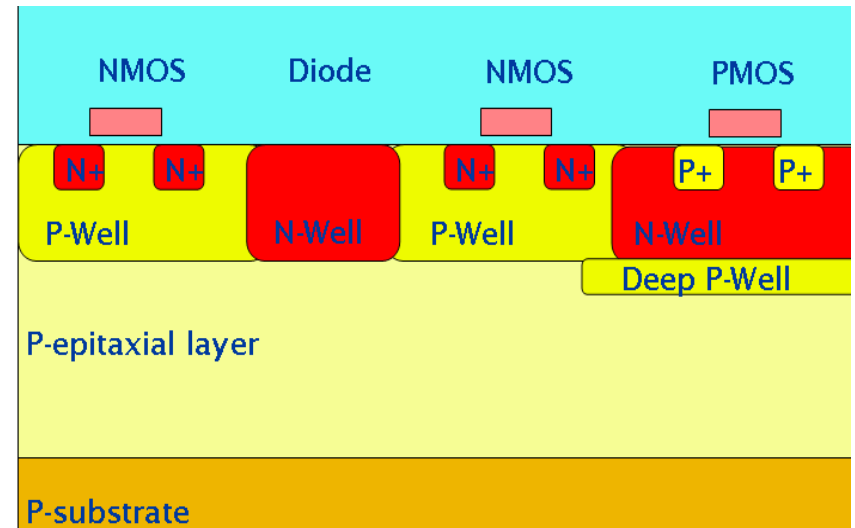
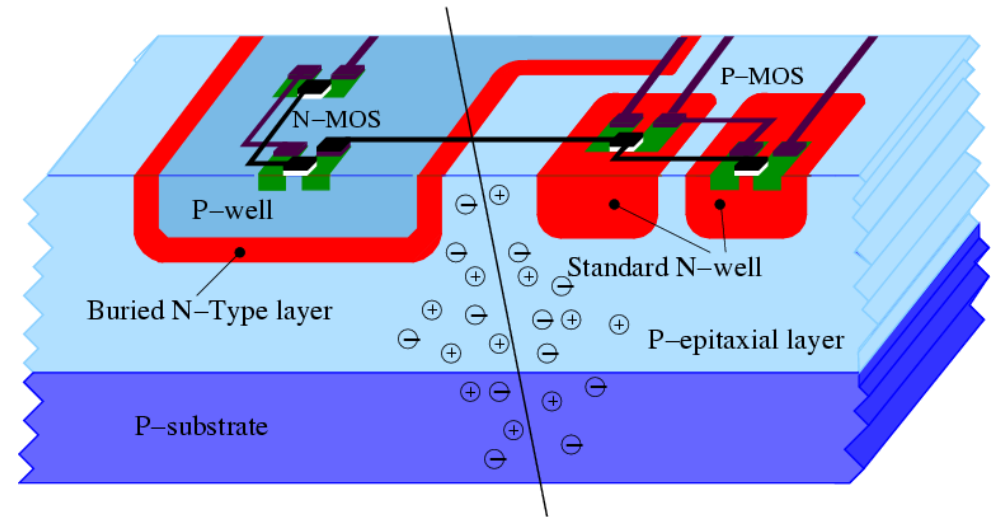
LDRD (LBNL et. al.)

- Current: LDRD03
 - 3T with in-pixel “CDS”
 - Readout at the end of a column
 - Made in 0.35 μm AMS OPTO process
 - 20 μm Pixels
 - 96 columns with 96 pixels each
- Rolling-Shutter readout



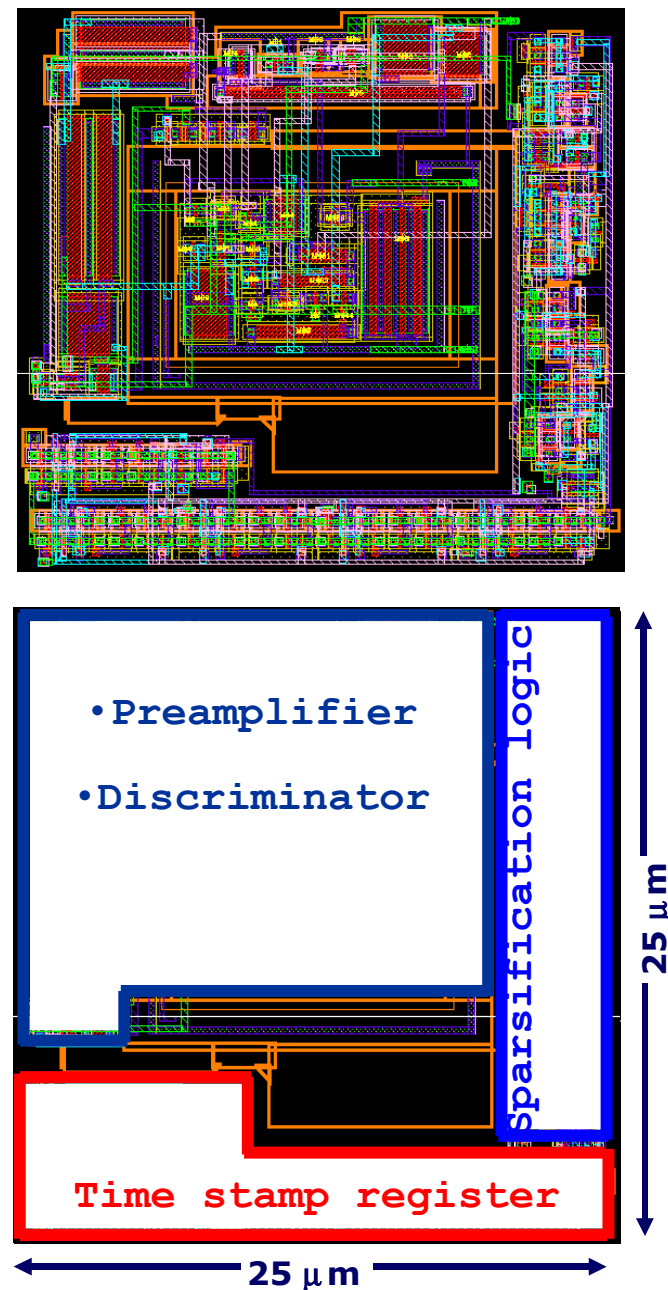
Overcoming the limits

- Two approaches
- Deep n-well
 - n-well diode as a deep implant covering most of pixel
 - Can have PMOS (small number)
- Deep p-well
 - Encapsulate electronics n-wells with deep p-implant
 - shielding, so no parasitic charge collection
 - Realized e.g. in INMAPS process and in ISIS



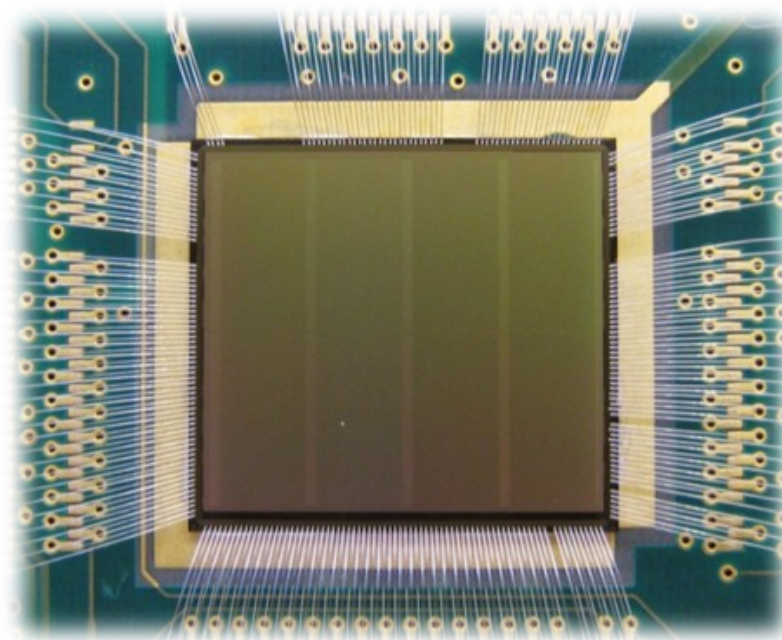
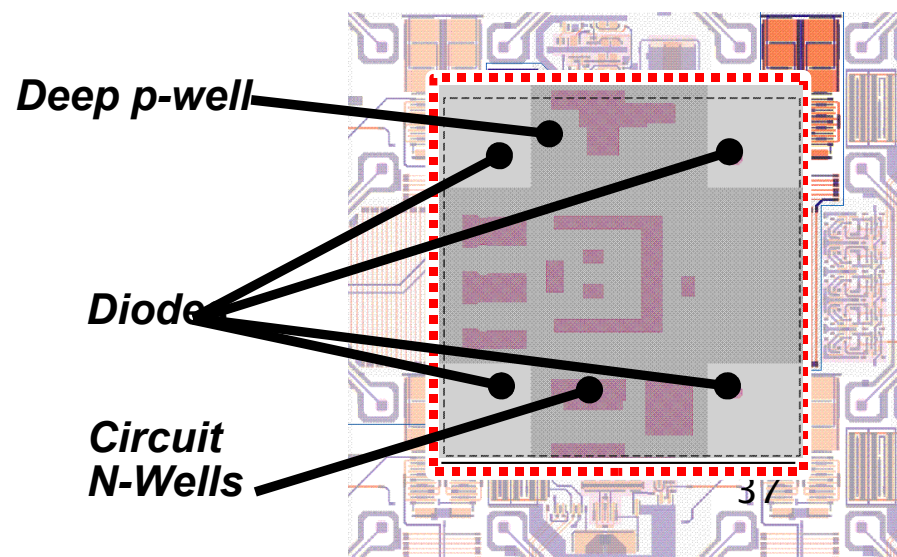
Deep n-Well MAPS (INFN)

- Made in ST 130 nm process
 - Triple-well approach
- 25 x 25 μm pixels with binary readout
 - Goal 15 x 15 μm
- Integrated electronics
 - Pre-amp, discriminator
 - Sparsification, time-stamping
- Plans to explore smaller feature sizes



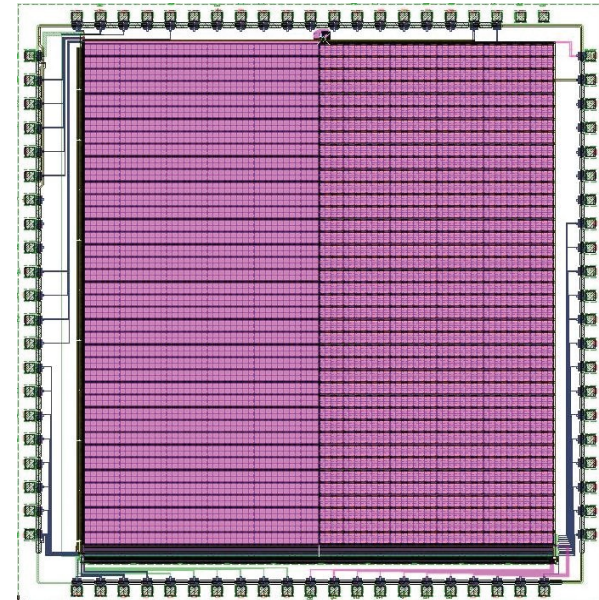
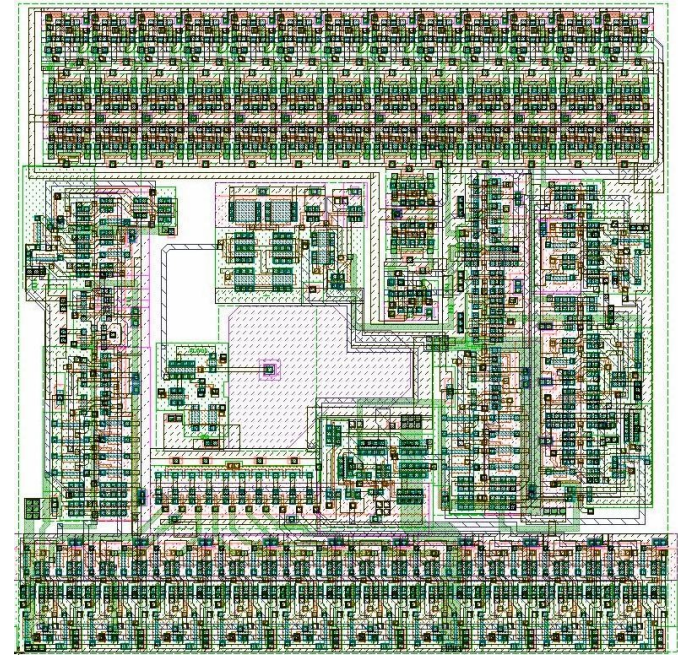
TPAC (CALICE-UK)

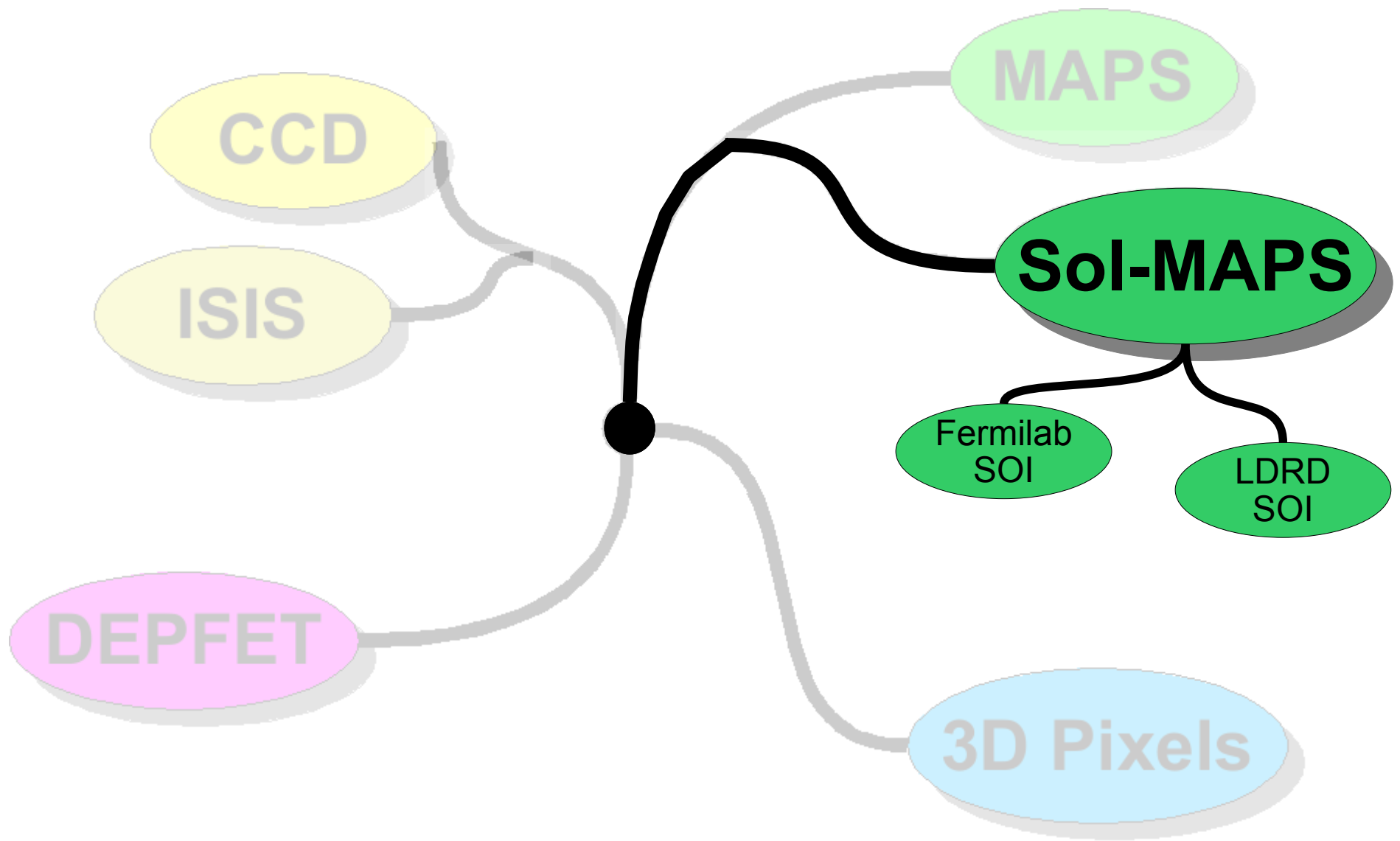
- 50 x 50 μm with binary readout
 - Deep p-well/INMAPS 180 nm
 - Pixel developed for digital EM calorimetry
 - Different optimization
- integrated electronics
 - Pre-amp, comparator
 - Pixel masks and trim
- Logic strips
 - Hold buffers and time-stamping
 - Add $\sim 11\%$ dead area



Chronopixels (Yale/Oregon)

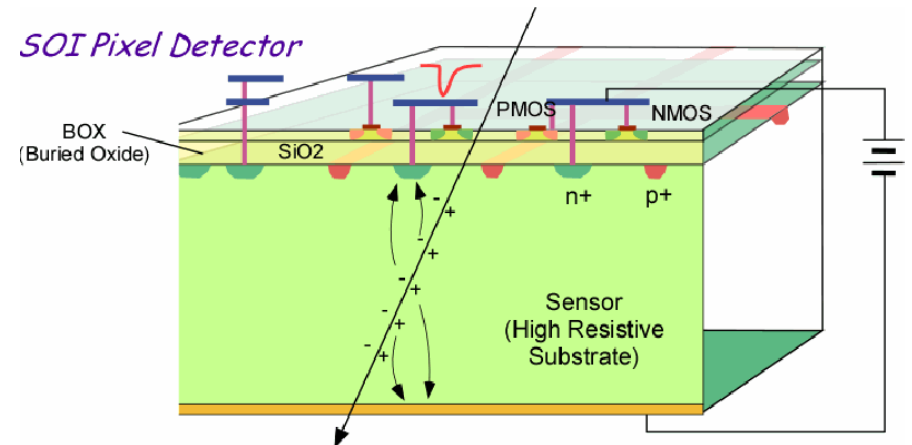
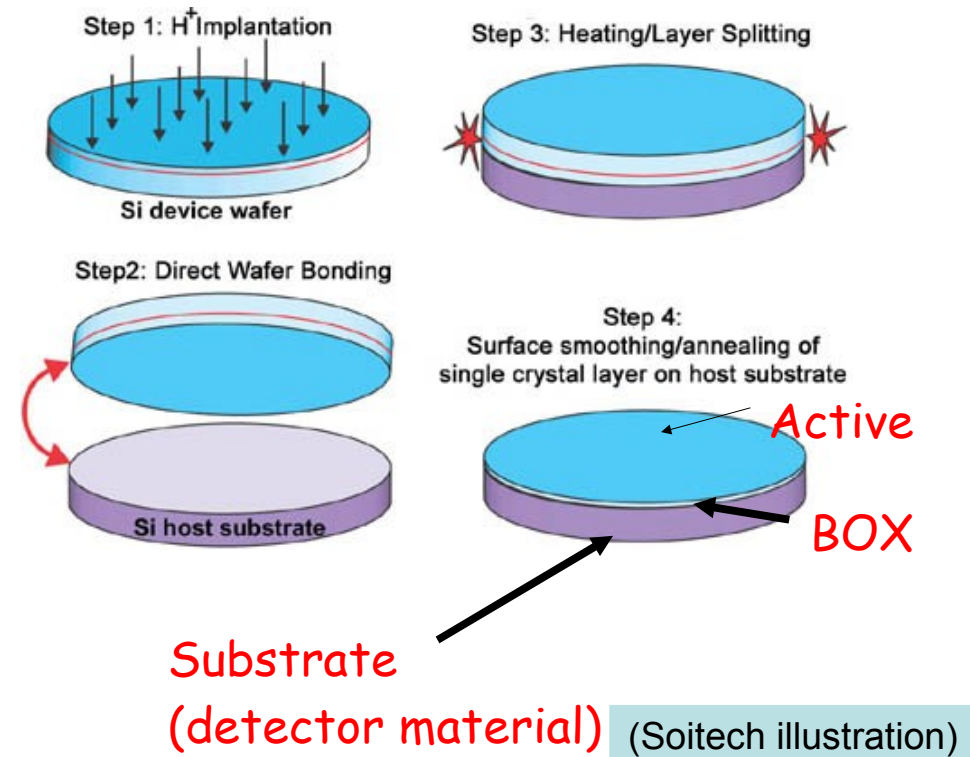
- Similar to previous pixels
 - In-pixel electronics
 - Hit buffering
 - Time-stamping
 - Binary readout
- Prototype made in 180 nm TSMC
 - Pixel size 50 x 50 μm
- Goal
 - 45 nm process
 - 10 x 10 μm pixels
 - Deep p-well and high-res epi





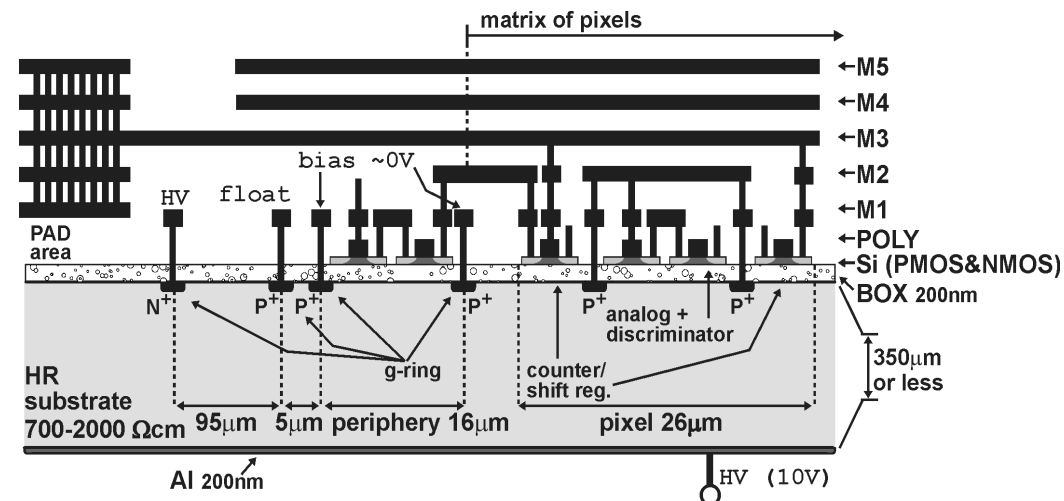
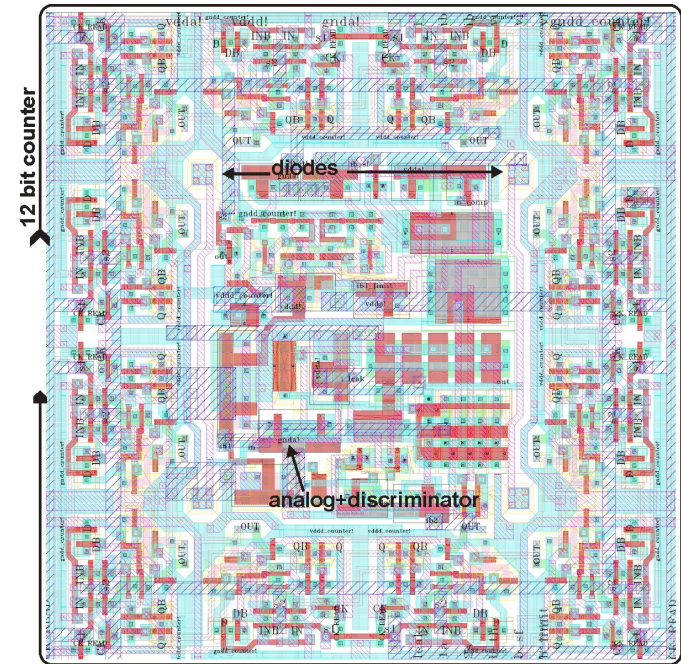
SoI Basics

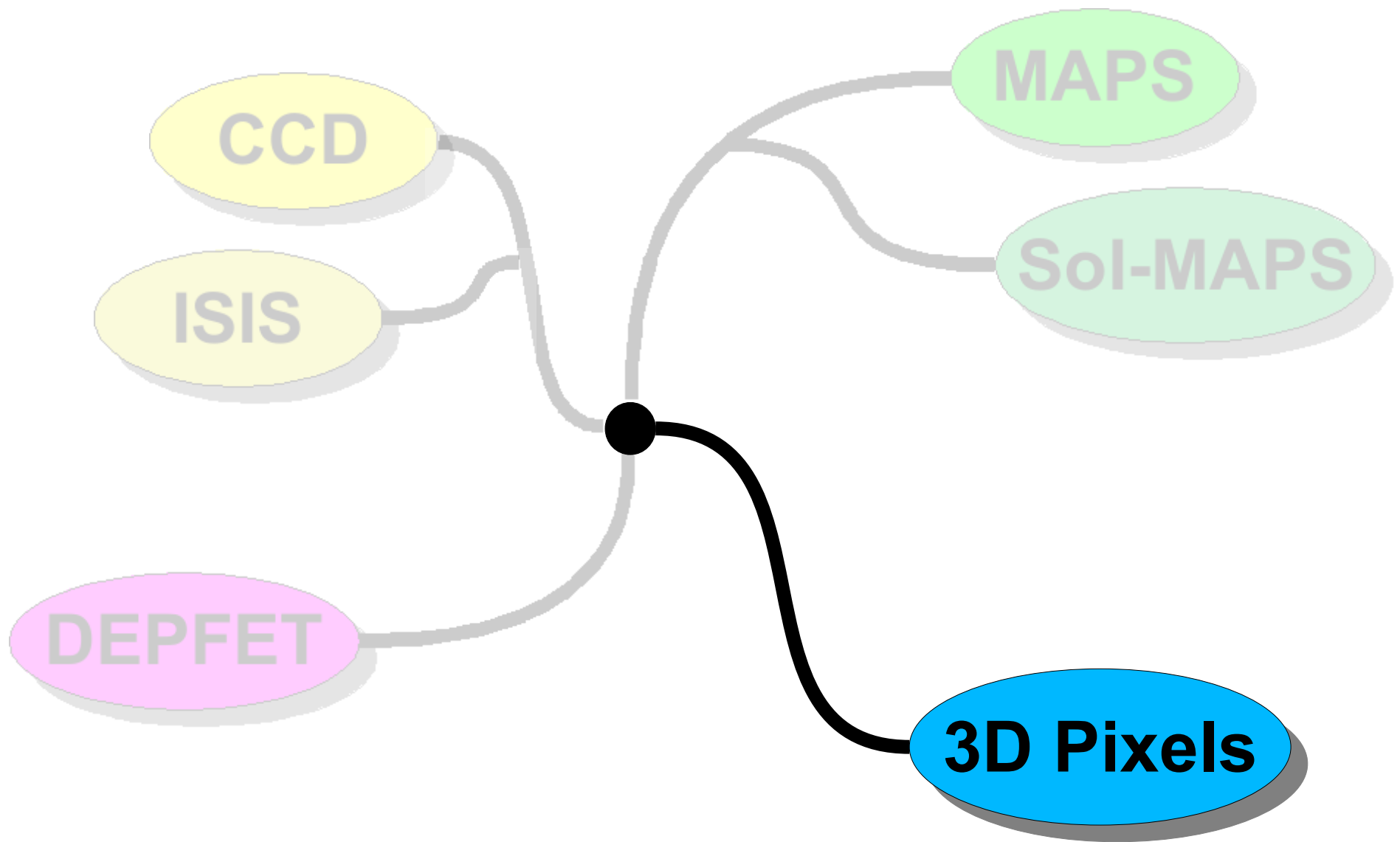
- **Silicon on Insulator (SoI)**
- Thin active circuit layer on insulating substrate
- ~200 nm of silicon on a “buried” oxide (BOX) carried on a “handle” wafer.
- Handle wafer can be high resistivity silicon
- Integration of electronics and fully depleted detectors in a single wafer
- Diode implant through the buried oxide



MAMBO (Fermilab)

- **M**onolithic **A**ctive pixel **M**atrix with **B**inary **c**ounters
- Made in 150 nm Oki Process
 - 200 nm BOX layer
- Pixel size is 26 x26 μm
 - Implements a 12 bit counter
- Common problem for all SoI
 - Backgate effect handling wafer
 - Can be fixed by using thicker BOX layer
 - Alternatively design work-arounds

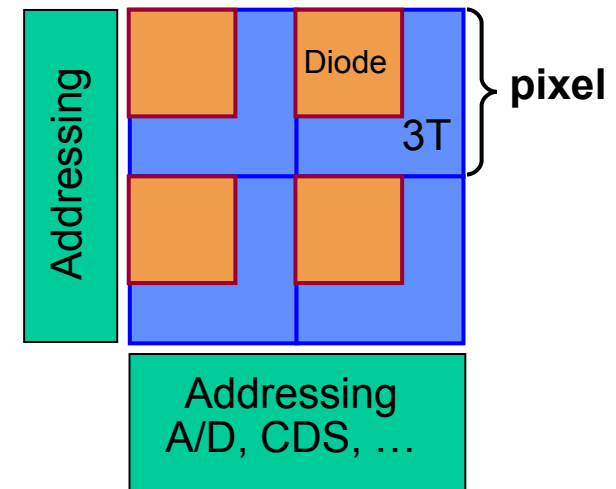




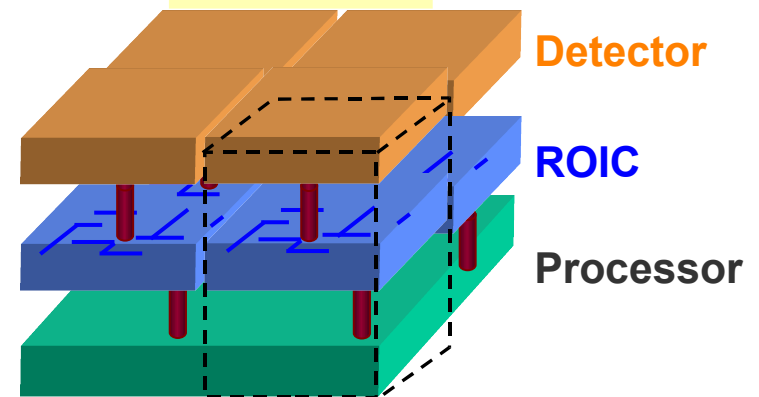
3D Pixels

- The ultimate dream of any pixel designer
 - Fully active sensor area
 - Independent control of substrate materials for each of the tiers
 - Fabrication optimized by layer function
 - In-pixel data processing
 - Increased circuit density due to multiple tiers of electronics
- A new way of doing things

Conventional MAPS

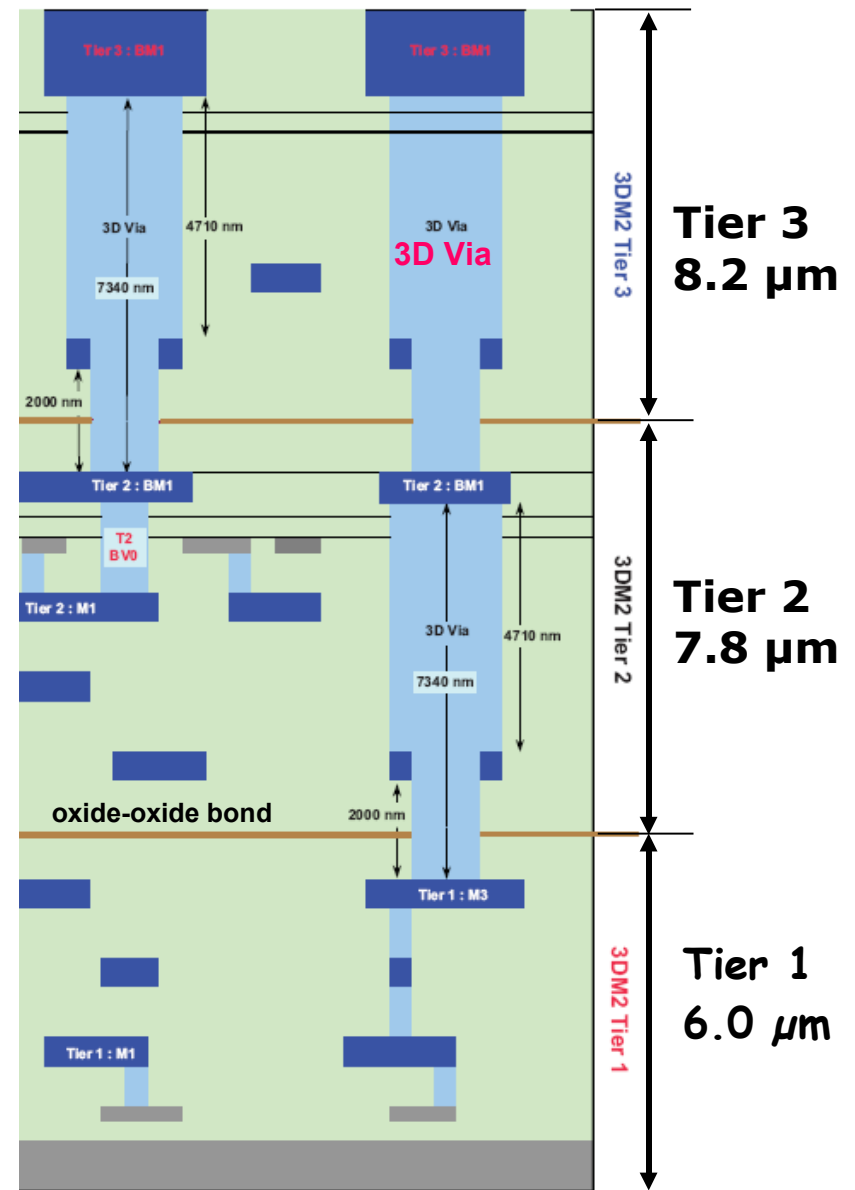


3-D Pixel



VIP-I (Fermilab)

- **V**ertically **I**ntegrated **P**ixel
- Pixel array 64x64, 20x20 μm pixels
 - Analog and binary readout
 - 5-bit Time stamping
 - Sparsification
- Designed for 1000 x 1000 array
- Chip divided into 3 tiers
- Made in MIT-LL process
- VIP2a is on its way



3D Process Developments

- The MIT LL process
 - Demonstrated a fully functional device
- However:
 - Poor yield- both processing problems and overly aggressive design
 - VIP2 will use degraded design rules (0.15 \rightarrow 0.2 or 0.3 μm) with improved transistor models
 - Analog SoI design is challenging
 - Long turn-around time
 - Not a commercial process
- Tezzaron 130 nm
 - Existing rules for vias and bonding
 - Relatively fast turn around
 - One stop shop for wafer fabrication, via formation, thinning, bonding
 - Low cost
 - Process is available to customers from all countries

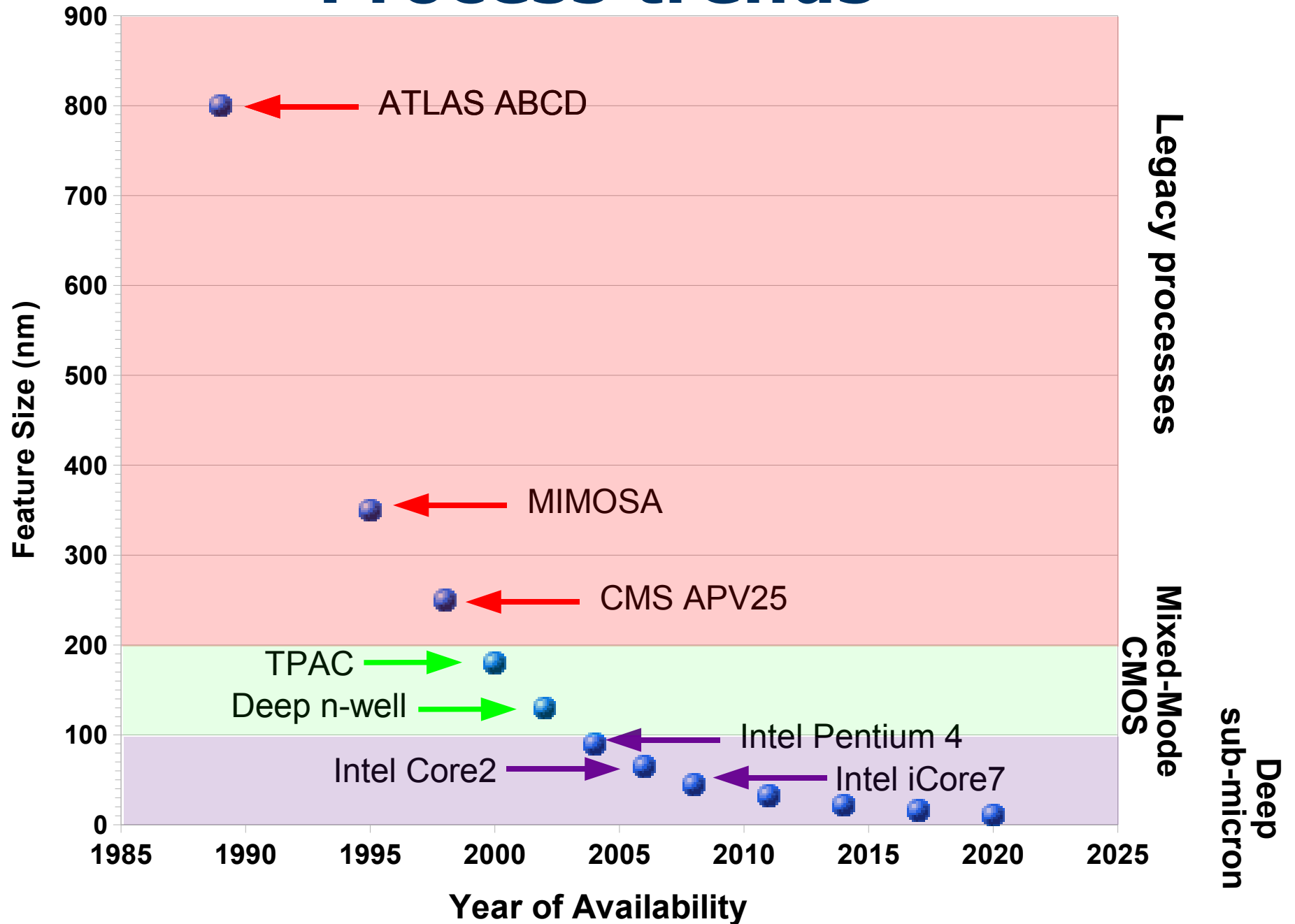


Future Trends

- *Always in motion the future is ...*
 - especially for pixels
- **Higher integration**
 - Smaller feature sizes and 3D integration will make this possible
- **Larger sensor areas**
 - Real CMOS Stitching allow wafer-scale sensors
- **Low power designs**
 - Large pixel system will need to reduce power usage per channel



Process trends

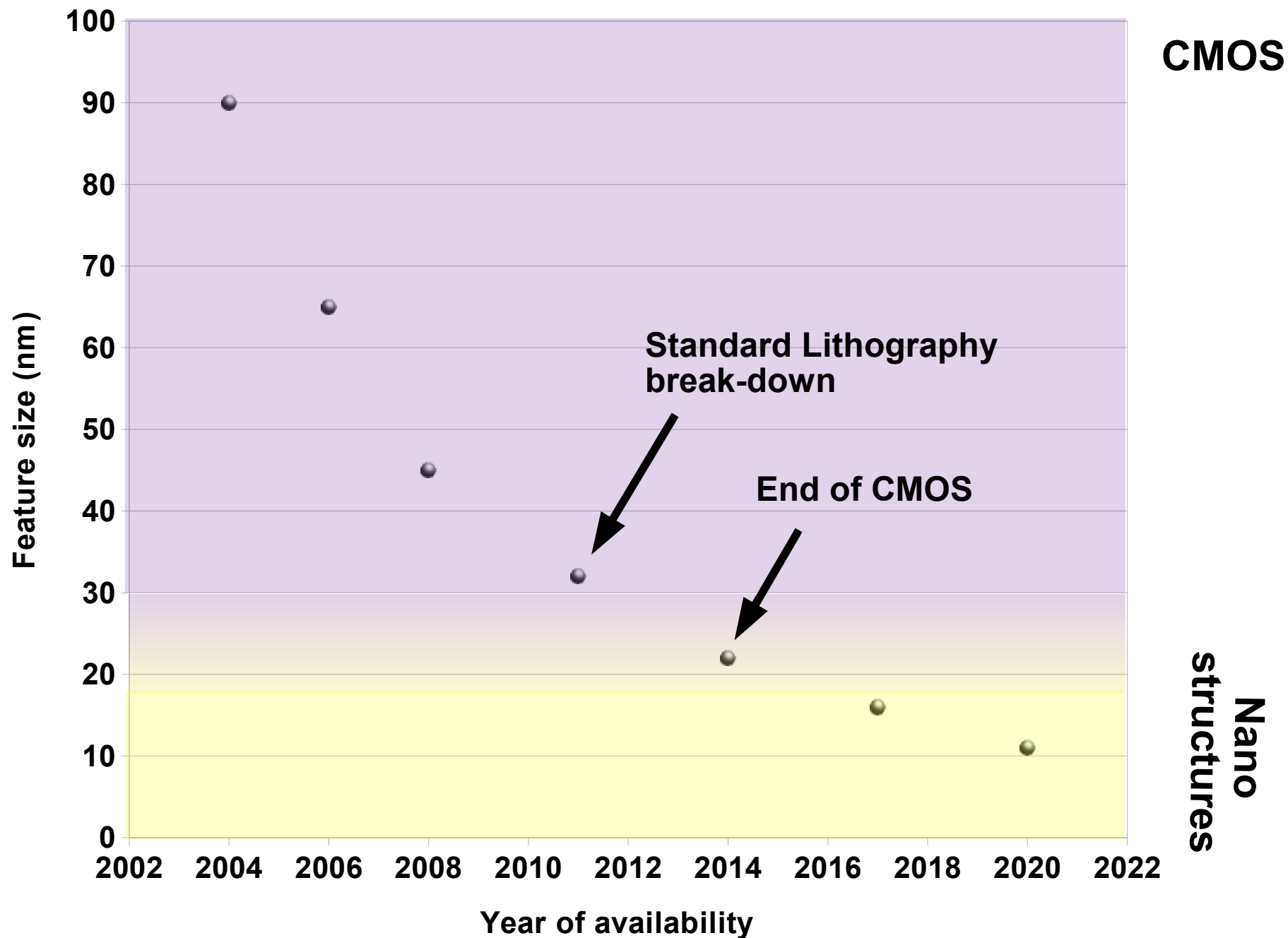


Why not deep submicron ?

- Some problems
 - Mostly pure digital processes (CPU, DRAM, etc)
 - Leakage Currents become a problem
 - small dynamic range due to operating voltage of 1 V
 - ADC design becomes way more difficult
 - New design kits, tools etc
 - Smaller process does not automatically mean smaller pixels
- Access to deep submicron processes
 - Very difficult, foundries are not keen on a runs with a few wafers only
 - Costs are not compatible with STFC funding
 - 180 nm mask set (~ 50.000 US-\$)
 - 65 nm mask set ($1.000.000$ US-\$)



Where does it end ...

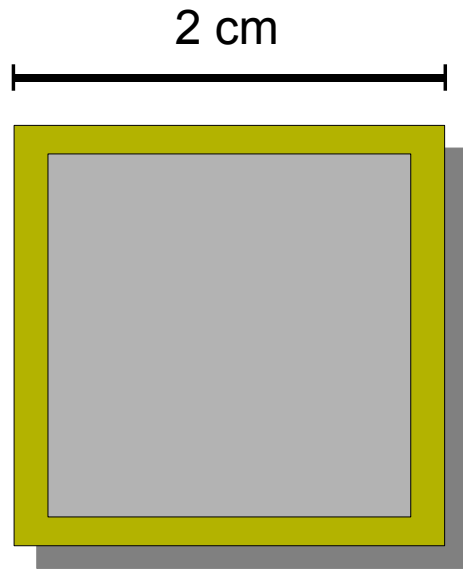


Large CMOS sensors

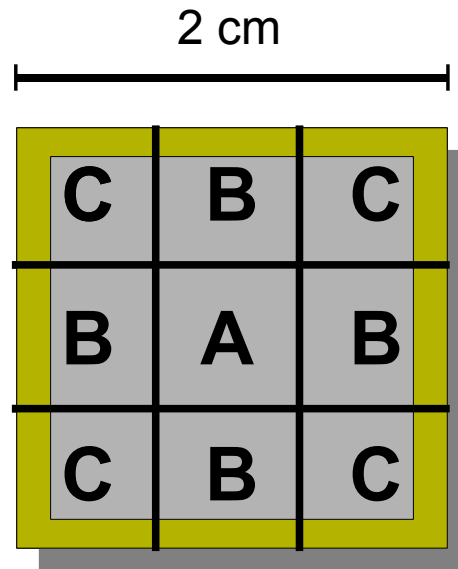
- CMOS structures have size limits
 - the reticle size
 - process-dependent
 - usually 25x25 mm
- This is a technology limit for large sensors
- Mainstream Industry not very interested
 - e.g. Intel Core2 (65 nm) 12x12 mm
 - Only interesting for imaging applications
- Way out : Stitching sensors



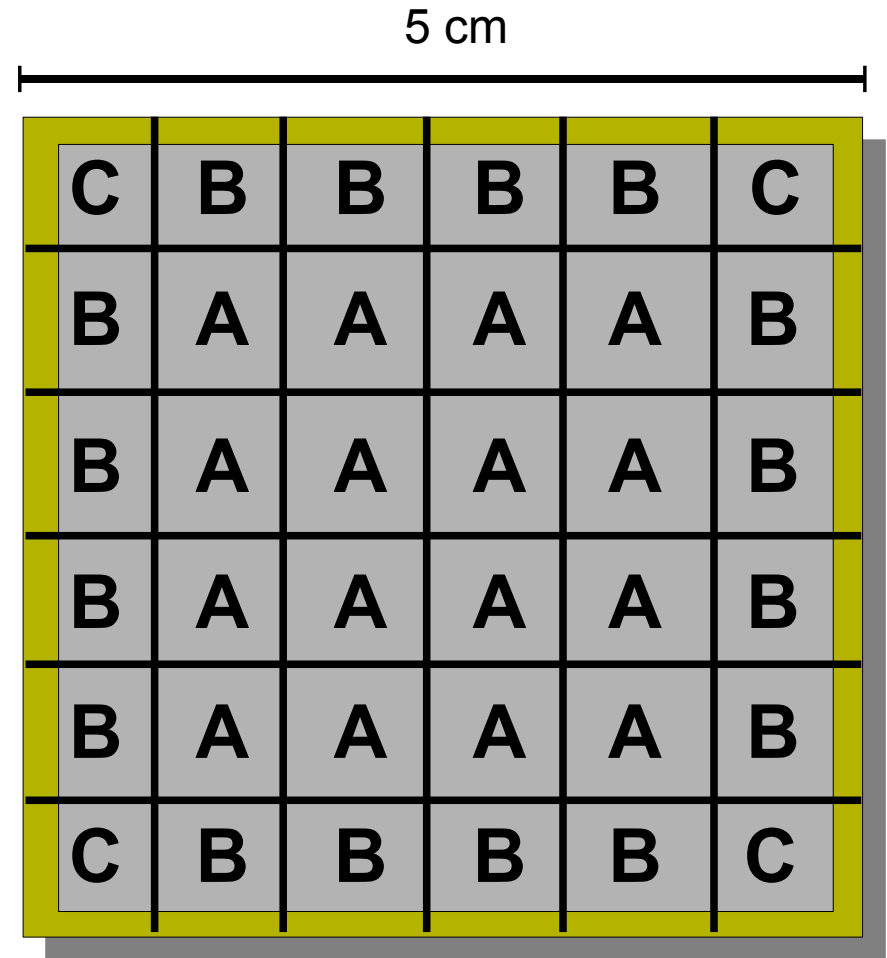
Stitching



Original
Sensor Design



Stitchable
Sensor Design



Stitched
Sensor Design

Some comments

- Stitching can't be a second thought
 - design for it from beginning
- Stitchable designs are more complex
- Mask set more expensive ..
- But then
 - normal wafer costs
 - mass producible
 - wafer size (300 mm) is the limit
- Caveat
 - larger structures mean lower yield ...
 - Compensate by robust/simple designs



Which Technology to choose?

- Even more difficult to make a forecast
- For a vertex detector
 - Small area ($\sim 1 \text{ m}^2$) so choose technology that can do the job
 - Cost is a minor issue
- For Silicon Pixel Trackers/ECAL etc
 - Industrial processes
 - Mass producible and cheap (large areas)
 - Minimize interconnects
- Interesting times ahead ...



SPiDeR

- CALICE-UK and LCFI got canceled by STFC
 - despite being major players in the pixel world
 - big innovations
- UK Pixel Community made a new proposal
- SPiDerR (**S**ilicon **P**ixel **D**etector **R**&D)
 - Birmingham, Bristol, Imperial College, Oxford and RAL
- 3 year Program
 - *Generic* Pixel R&D (TPAC, Novel Structures)
 - *Generic* Techniques using Pixels (DECAL)
 - ISIS support was canceled by STFC



Summary

- If you like to know more ...
 - The ILC R&D reviews are an excellent summary of the activities
 - http://www.linearcollider.org/wiki/doku.php?id=drdp:drdp_home
- Thanks to
 - J. Brau, C. Damerell, M. Demarteau, T. Greenshaw, L. Linssen, R. Lipton, K.D. Stefanov, Y. Sugimoto, R. Turchetta, M. Tyndel, N. Wermes for material, comments and discussion



Who is doing what

- LCFI (UK collaboration)
 - CPCCD/ISIS
- FPCCD group
 - FPCCD
- DEPFET Collaboration
 - DEPFET
- LBNL/INFN/Purdue
 - MAPS/SoI MAPS
- Fermilab
 - SoI MAPS/3D Pixels
-
- CALICE-UK
 - MAPS (TPAC)
- CMOS-VD
 - MAPS (MIMOSA)
- Hawaii
 - CAP

